

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **BLOCK DIAGRAM**
Pegatron Corp. Engineer: **Vic_Chen**

Size A3	Project Name IPMIP-DP	Rev 1.01
Date: Friday, April 23, 2010	Sheet 1 of 68	

Schematics Change History

[illegible]

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

PEGATRON DT-MB RESTRICTED SECRET

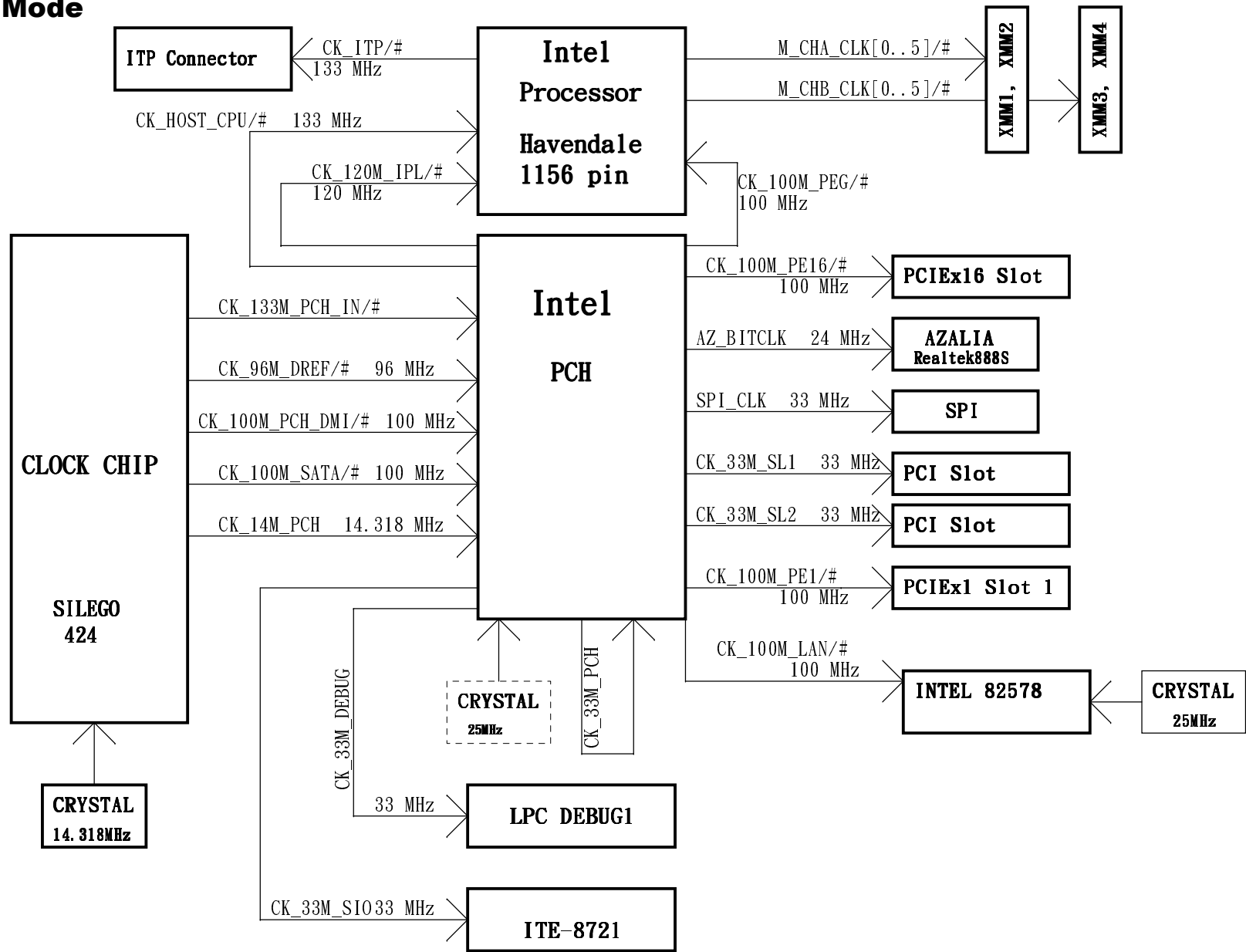
PEGATRON Title : **CHANGE HISTORY**

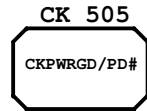
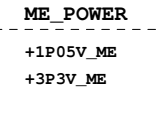
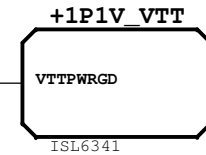
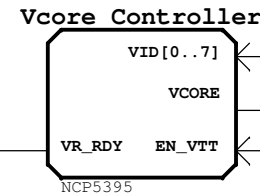
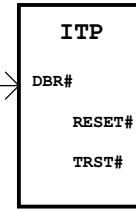
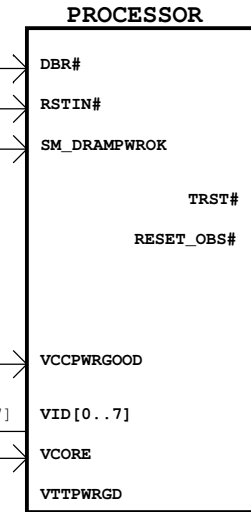
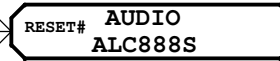
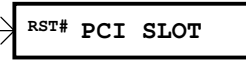
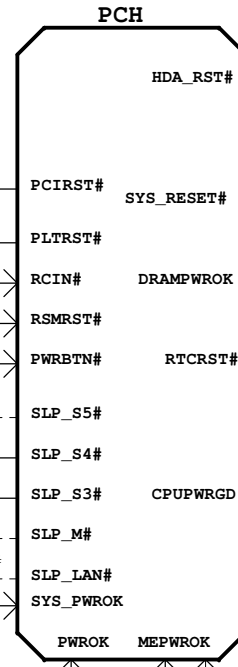
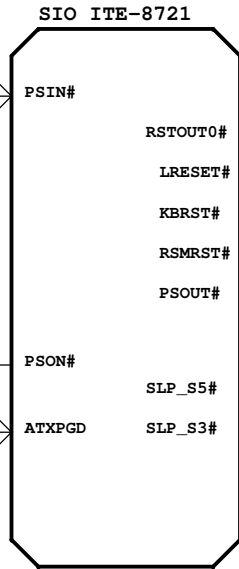
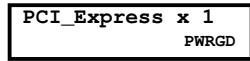
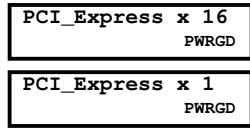
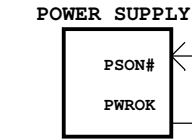
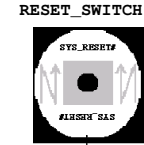
Pegatron Corp. Engineer: Vlc_Chen

Size	Project Name	Rev
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A3	IFMIF-DF	1.01
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PCH Buffer Mode





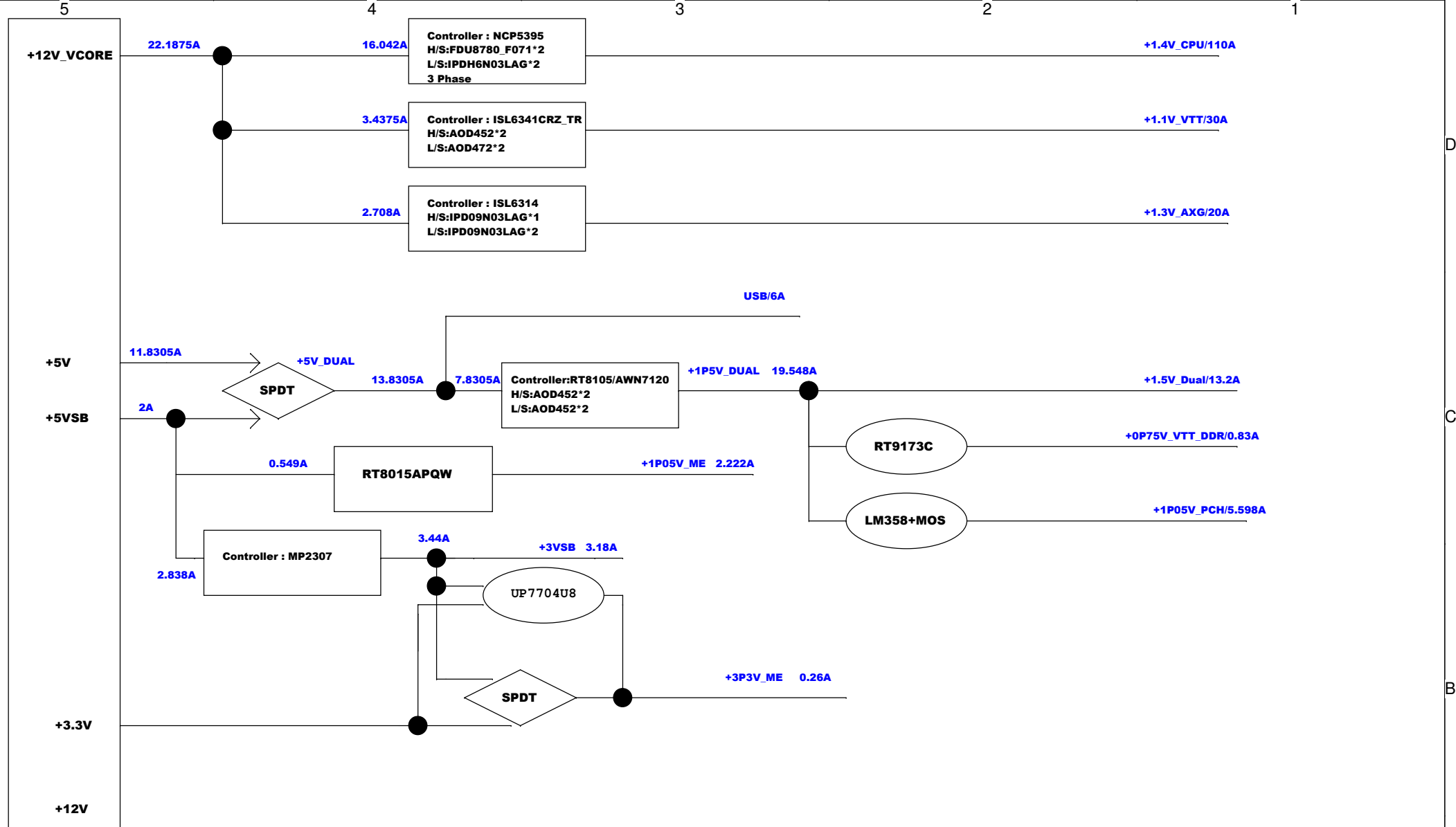
If support AMT, SLP_M#
will come with SLP_S5

If not support AMT, SLP_M#
will come with SLP_S3



CHIP

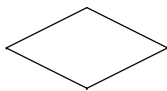
SOCKET or SLOT



SWITCHING



LINEAR



SWITCH ON/OFF

<Variant Name>

PEGATRON		Title : POWER FLOW	
PEGATRON CORPORATION		Engineer: Michael Lee	
Size A3	Project Name IPMIP-DP		Rev 1.01
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	Lynnfield/Clarkdale
VCORE	-> 90A - 95(TBD)W
+1.1V_VTT	-> 30A(TBD) - 33W
+1.5V	Vddq -> 6A - 9W
+1.8V	Vccpll -> 1.35A - 2.43W

	Intel Ibox Peak
V_CPU_IO	-> <1mA - 1.1mW
+5V	V5REF -> <1mA - 5mW
+5V	V5REF_Sus -> <1mA - 5mW
+3.3V	Vcc3_3 -> 0.357A - 1.178W VccDAC -> 0.069A - 0.228W
+1.1V	VccDMI -> 0.065A - 0.07W
+1.05V	VccADPLL -> 0.075A - 0.079W VccADPLLb-> 0.075A - 0.079W VccCORE -> 1.629A - 1.71W VccIO -> 3.251A - 3.414W VccLAN -> 0.372A - 0.39W VccME -> 2.222A - 2.333W
+1.8V	VccqNAND -> 0.156A - 0.281W VccVRM -> 0.196A - 0.353W VccTX_LVDS -> 0.059A - 0.106W
+3P3V	VccALVDS -> <1mA - 3.3mW
+3P3VSB	VccRTC -> 2mA - 6.6mW VccSus3_3 -> 0.168A - 0.554W VccSusHDA -> 0.006A - 0.02W VccME3_3-> 0.086A - 0.284W

	CLOCK- CK505
+3P3V	-> 250mA - 0.825W
+VDD_IO (0.8V)	-> 80mA - 64mW

	DDR3 DIMM (4) & Termination
+1.5V_DAU1	VDD (S0, S1) -> 7.2 A - 10.8W VDD (S3) -> 712mA - 1.07W
SM_VTT(0.75V)	SM VTT (S0, S1) -> 0.83A - 0.623W

	PCI Express x 1
+12V	-> 0.5A - 6W
+3P3V	-> 3.0A - 9.9W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI SLOTS
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.6A - 25.08W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	INTEL 82578
+3P3V_CL	-> 15.5mA (TBD) - 51.15mW
+1P8VSB_LAN	-> 300mA - 540mW
VCC_LAN(1.05V)	-> 300mA -315mW

	S10 ITE-8721
+5V	-> 1mA - 5mW
+3.3VSB	-> 2.4uA - 7.92uW
+3.3V	-> 2mA - 6.6mW

	ALC888S Azalia Codec
+5VSB	-> 0.6A - 3W
+3P3V	-> 0.4A - 1.32W

	USB 12 PORTS
+5V_DUAL	(S0, S1) -> 8.4A - 42W (S3) -> 0.336A - 1.68W

	1394A
+3P3V	-> mA - W

	HDMI
+3P3V	-> mA - mW
+2P5V_DVI	-> mA - mW

	SATA 6 PORTS
+5V	-> 0.975A - 4.875W
+12V	-> 0.9A - 10.8W

	FAN
+12V	-> 0.6A - 7.2W

	PS2 KB/MS
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW

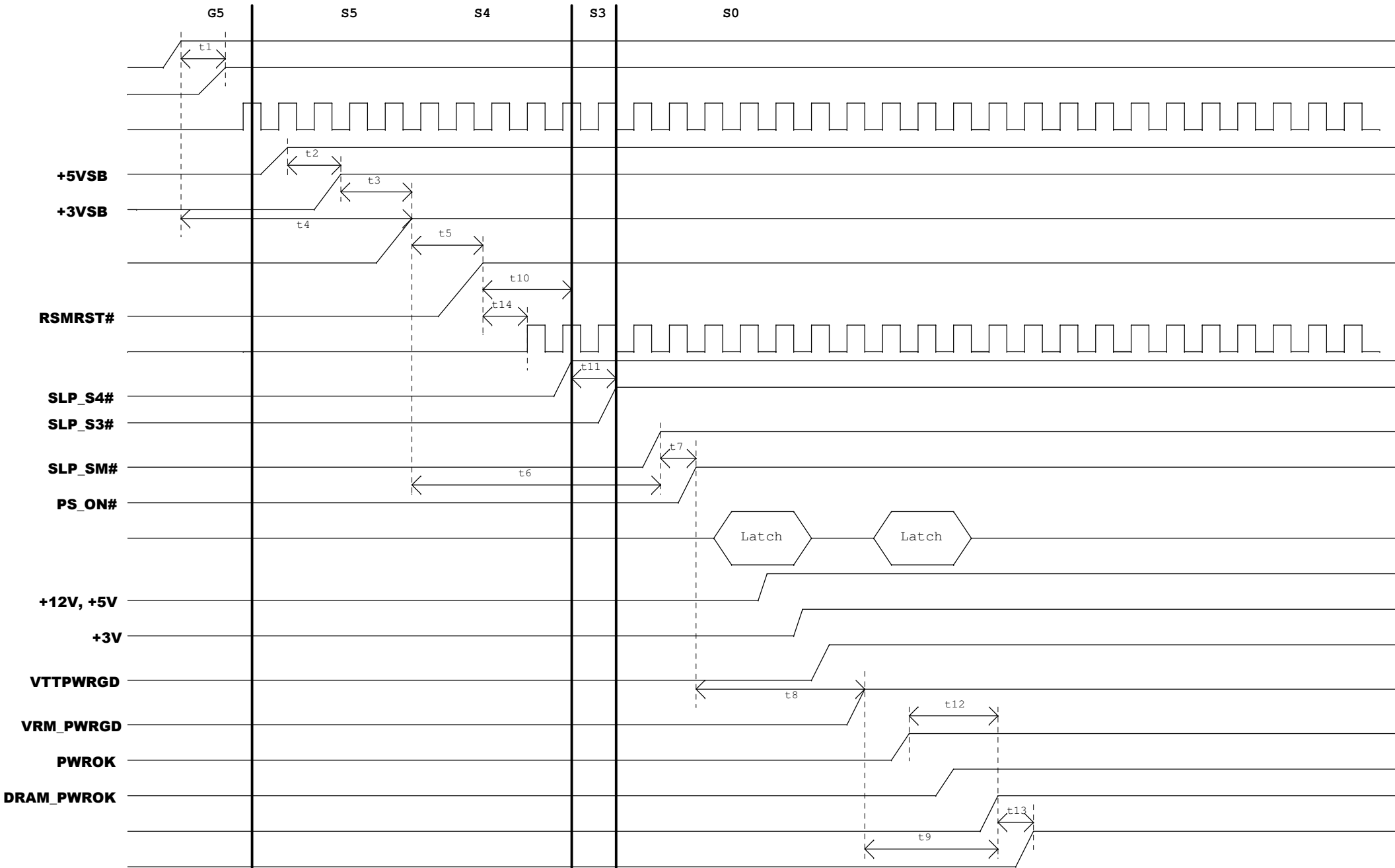
	SPI
+3V	-> 30mA - 99mW

	HDD
+12V	-> 0.75A - 9.0W
+5V	-> 0.75A - 3.75W

	CD ROM
+12V	-> 0.75A - 9.0W
+5V	-> 0.75A - 3.75W

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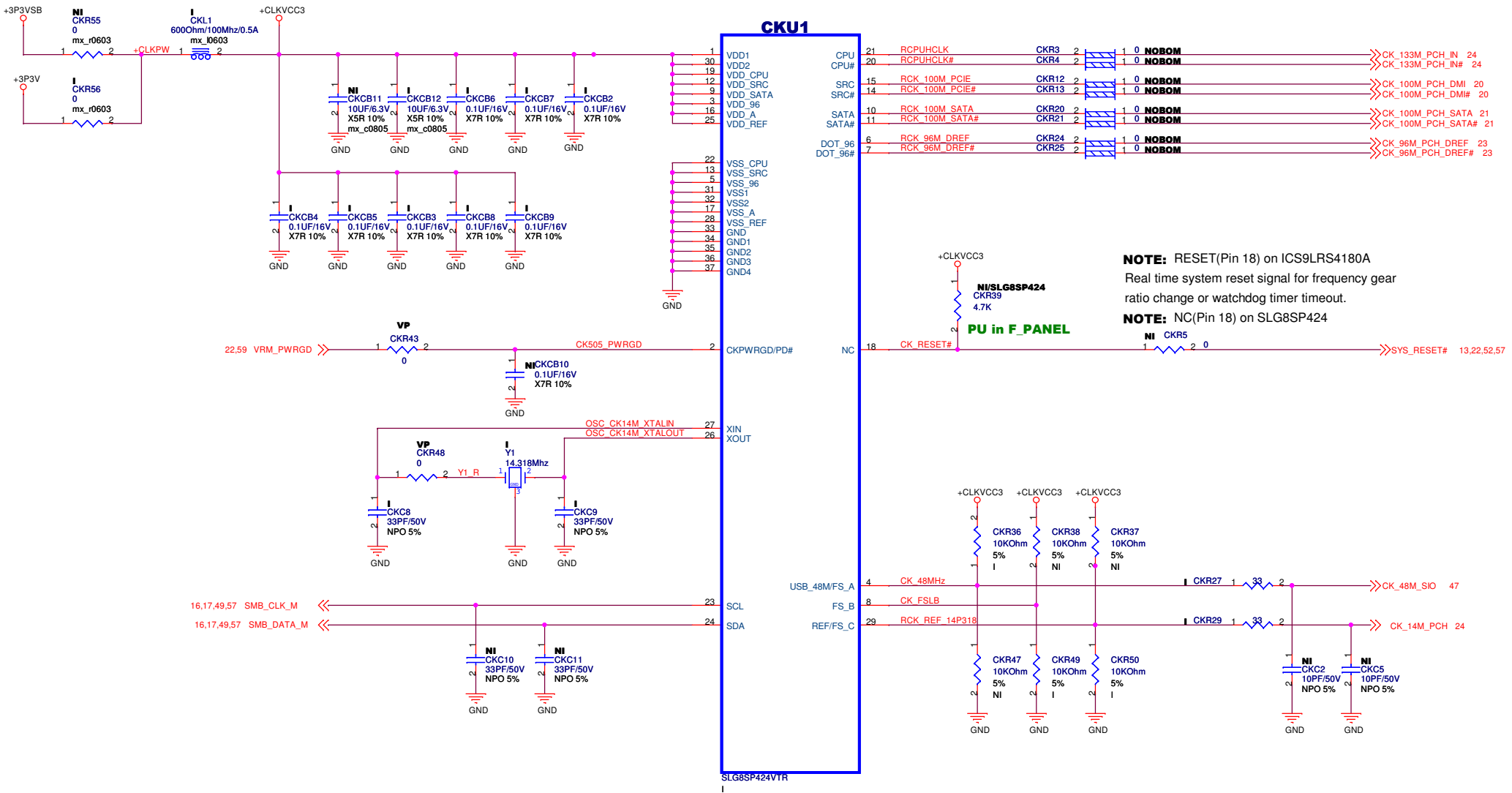
PEGATRON		Title : POWER DISTRIBUTION	
Pegatron Corp.		Engineer: Vic_Chen	
Size A3	Project Name IPMIP-DP	Rev 1.01	
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The data is not final

- t1>18ms
- t2>0ms
- t4>0ms
- t5>10ms
- t6>0ms
- t7>0ms
- t9>99ms
- t10<110ms
- t11>1RTCCLK
- t12>5ms
- t13:35~74RTCCLK
- t14<110ms

ICS9LRS4180AKLFT: 0610-0038000
SLG8SP424VTR: 0610-007D000



NOTE:

FSLC	FSLB	FSLA	CPU FREQ
0	0	1	133MHz
1	0	1	100MHz

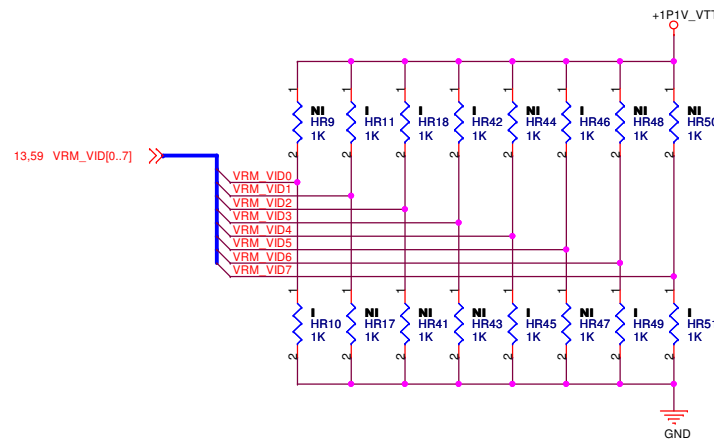
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : ICS 4180/SLG 424

Pegatron Corp. Engineer: Vic_Chen

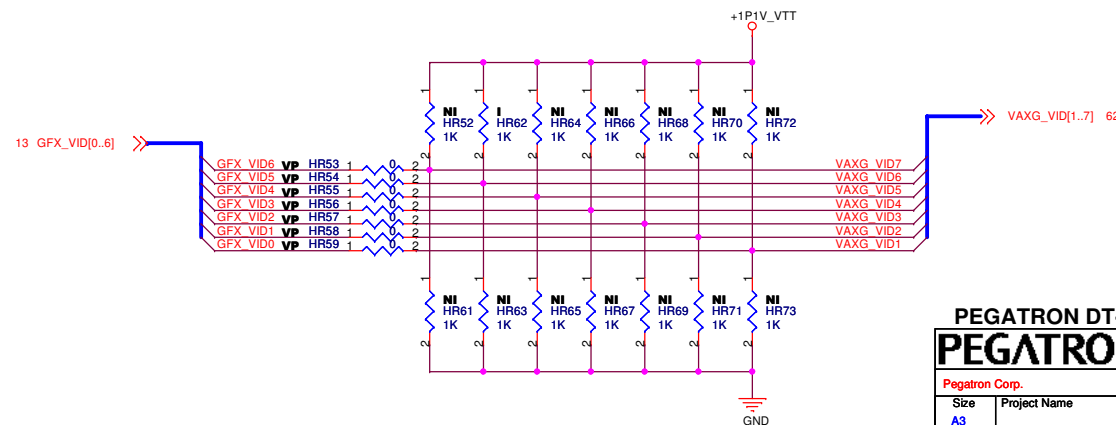
Size A3 Project Name IPMIP-DP Rev 1.01

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POWER ON CONFIGURATION (POC) TABLE

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG3	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW



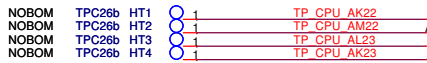
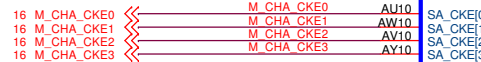
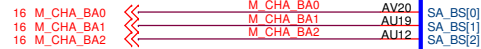
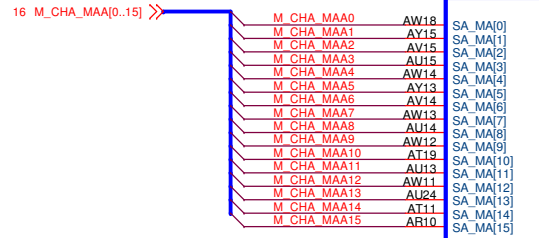
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VID RES

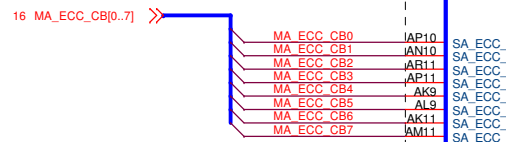
Pegatron Corp. Engineer: Vic_Chen

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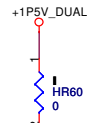
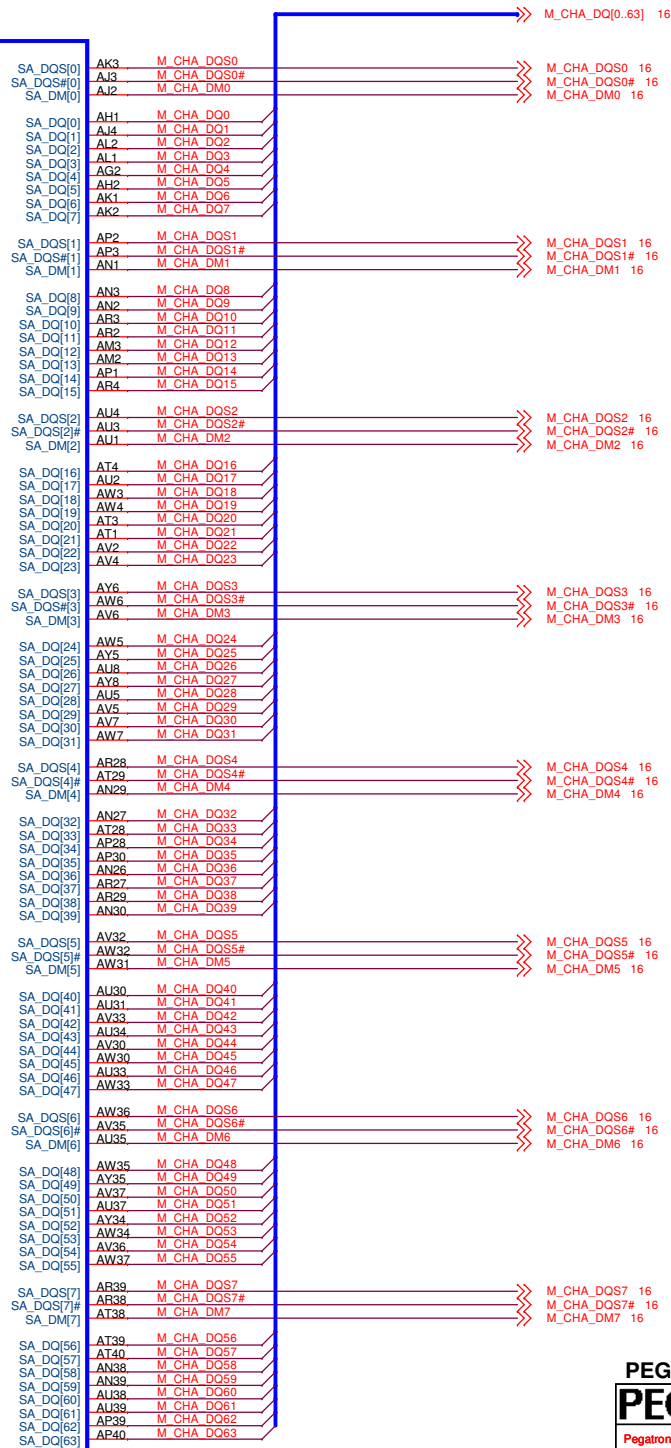
NOTE:
For ECC DIMM



HU1A

DDR_A

SOCKET_1156P



16,17 DDR3_DRAMRST# <<< AV8 SM_DRAMRST#

IP R1.02 added to reduce
The glitch.



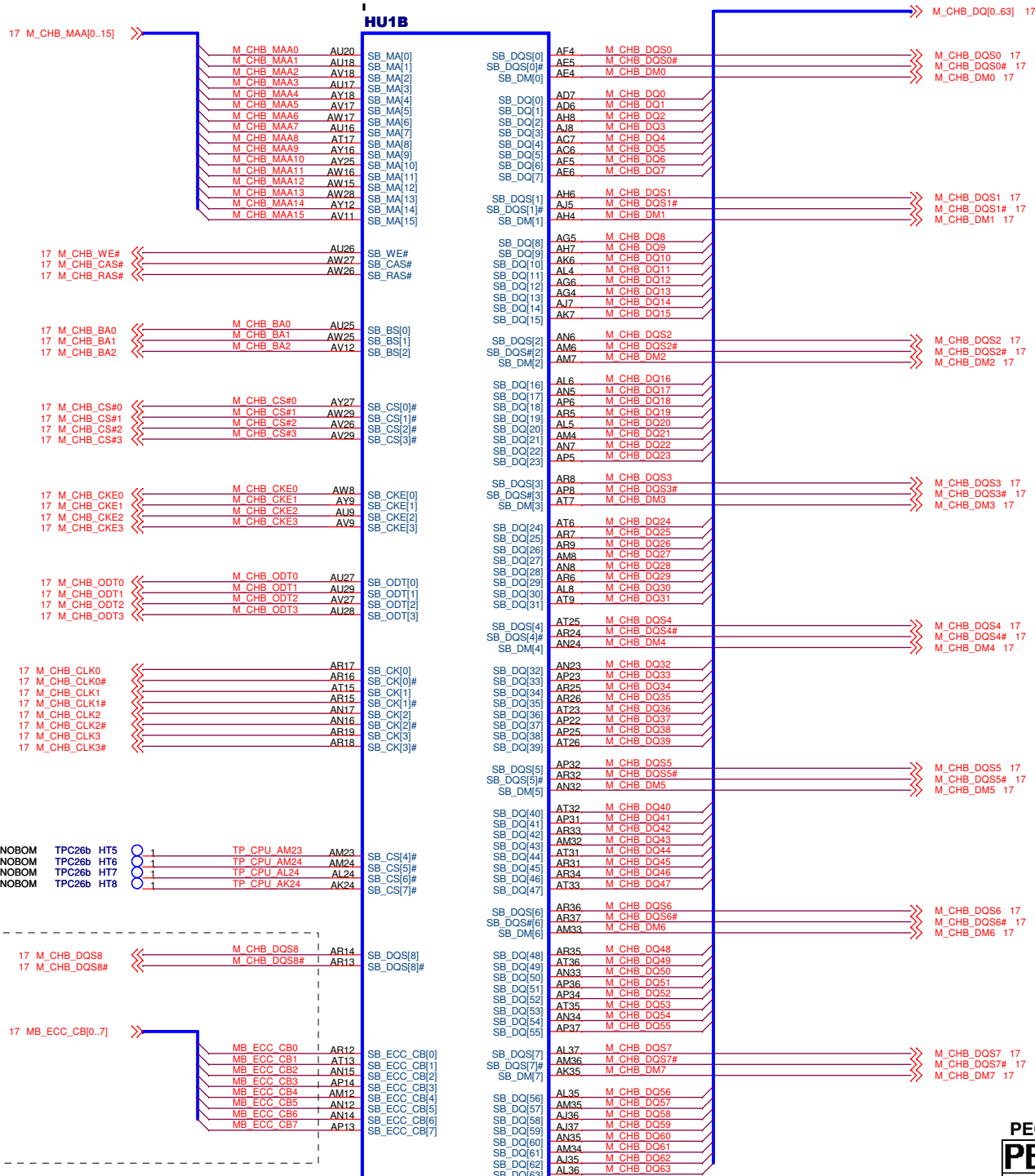
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 1

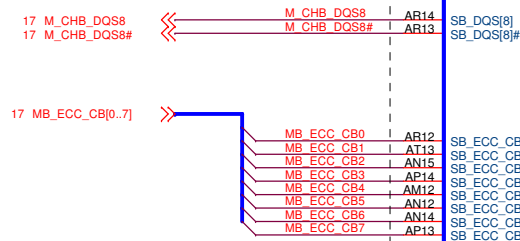
Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMP-IP Rev 1.01

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NOTE:
For ECC DIMM



DDR_B
SOCKET_1156P

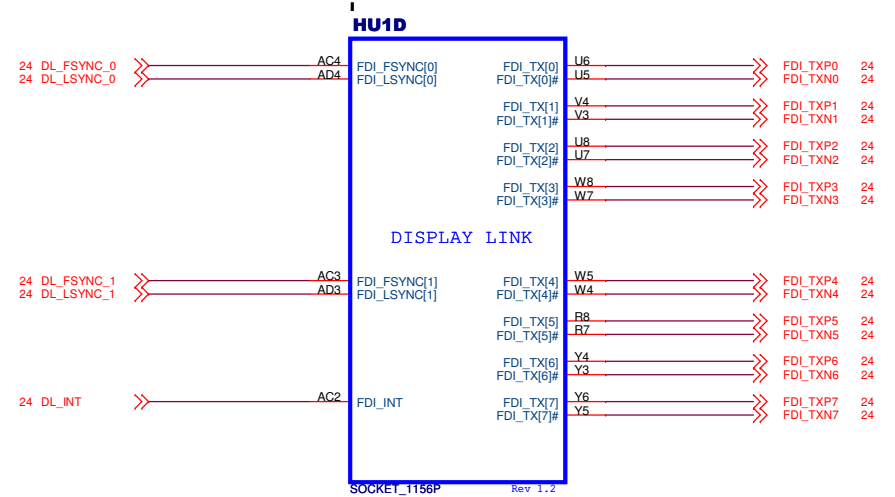
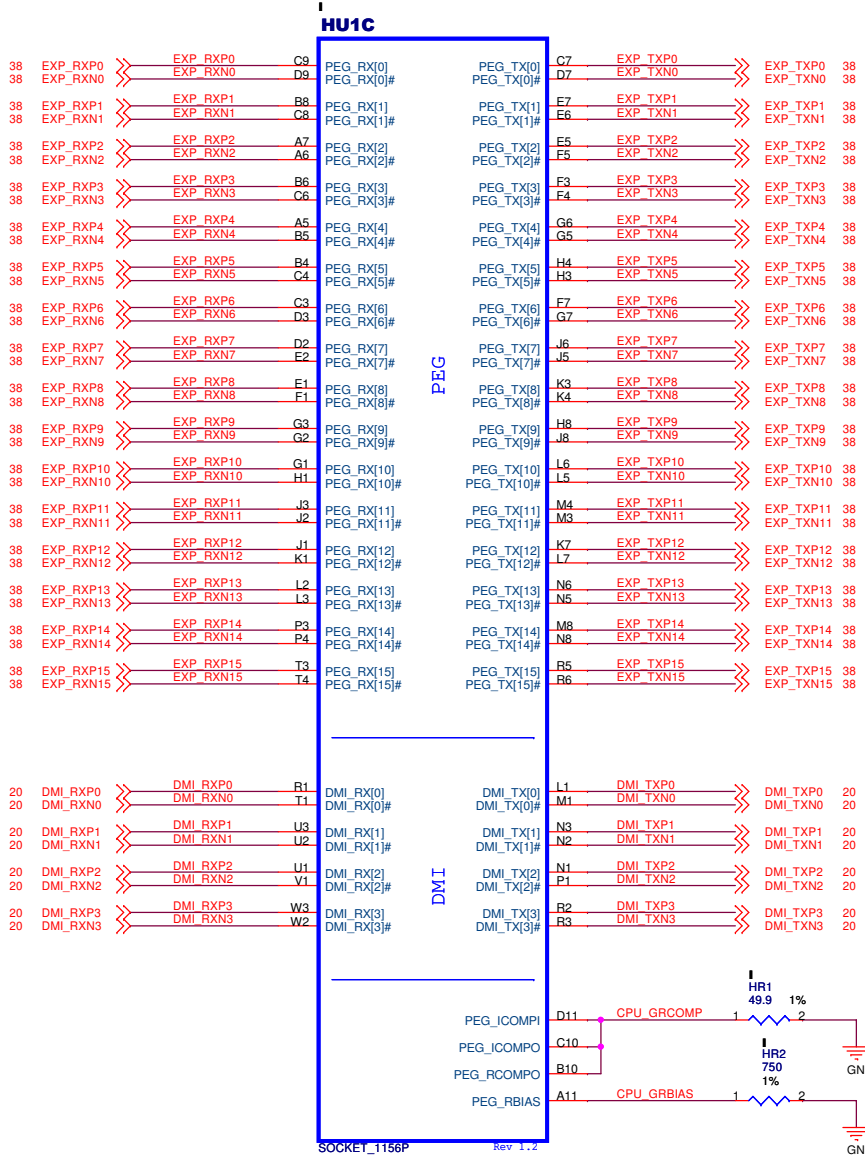
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 2

Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 11 of 68



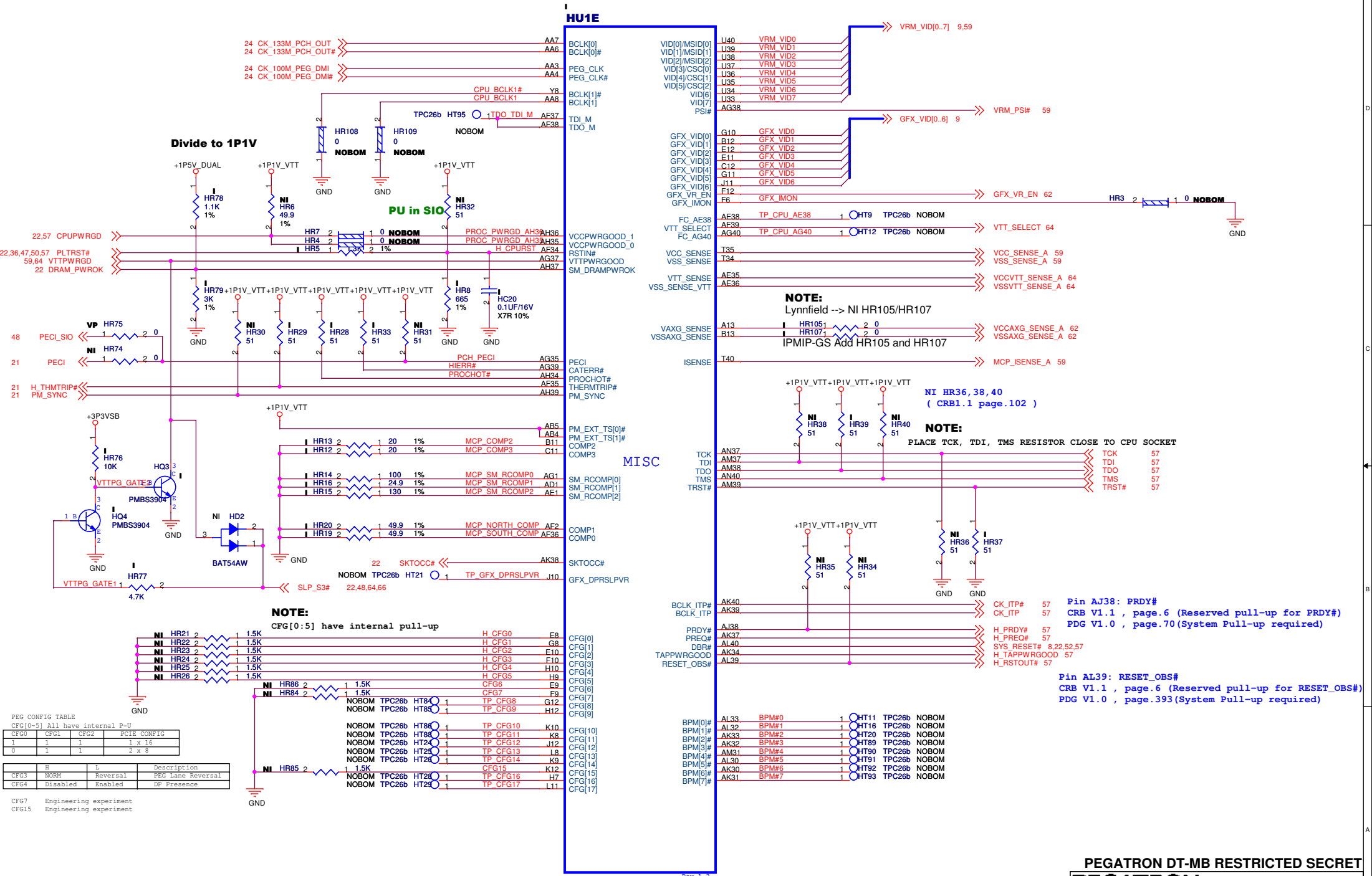
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 3

Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

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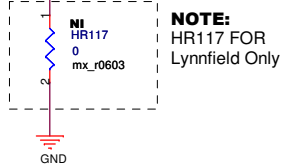
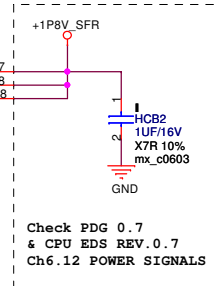
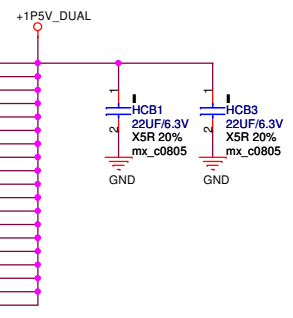
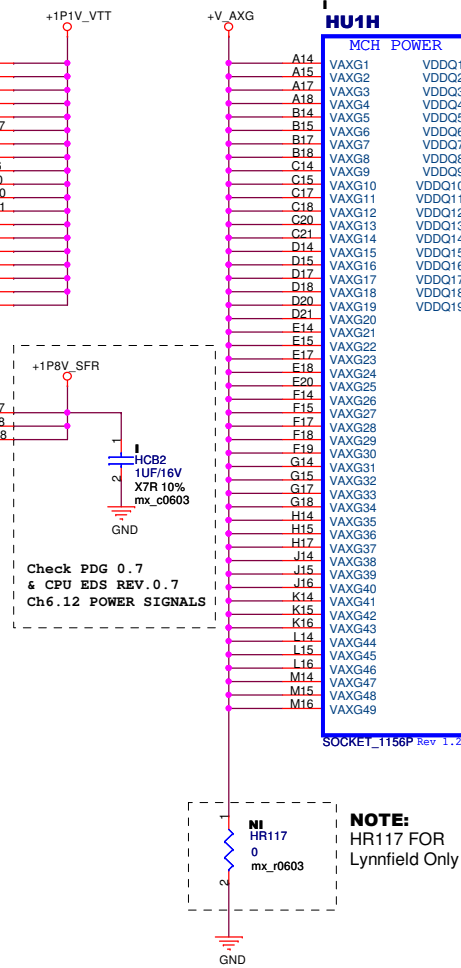
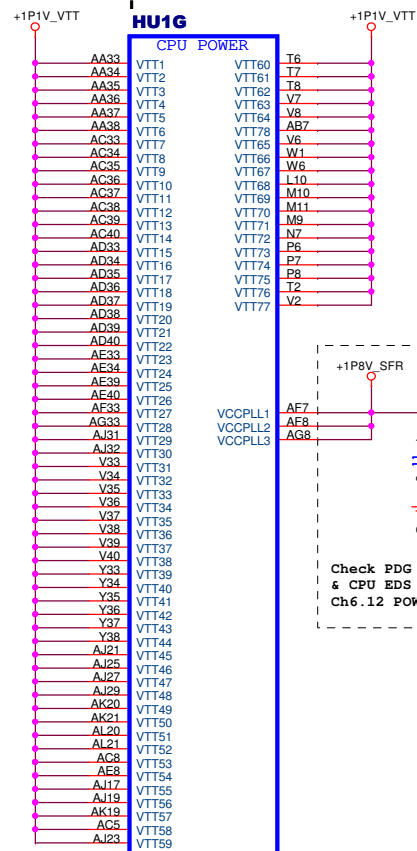
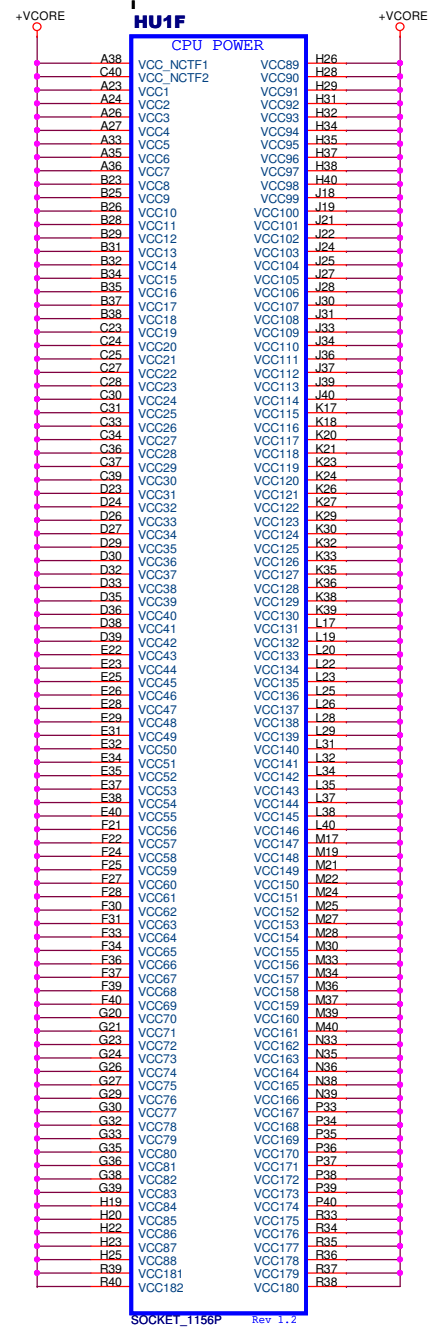
PEG CONFIG TABLE

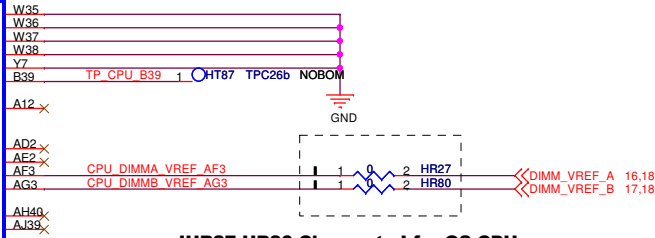
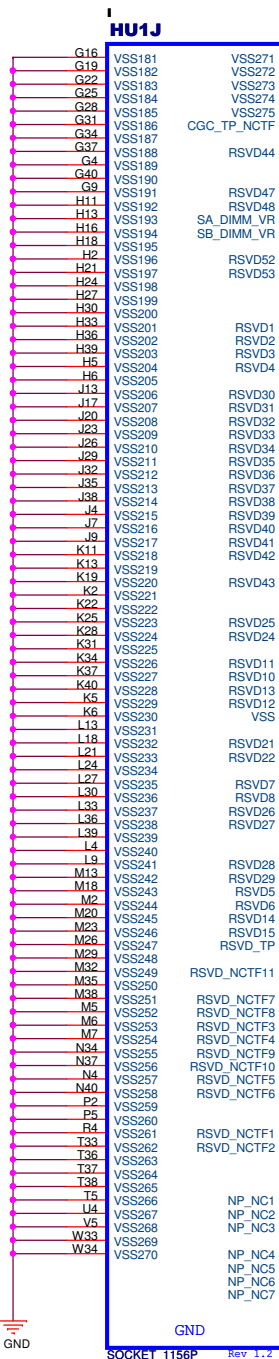
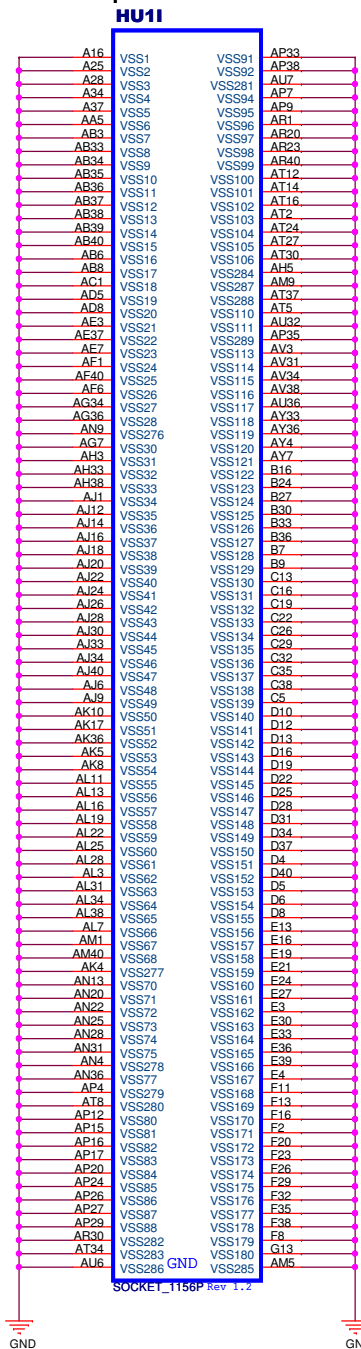
CFG[0-5] All have internal P-U

CFG0	CFG1	CFG2	PCIE CONFIG
1	1	1	1 x 16
0	1	1	2 x 8

B	L	Description
CFG3	NORM	Reversal PEG Lane Reversal
CFG4	Disabled	Enabled DP Presence

CFG7 Engineering experiment
CFG15 Engineering experiment

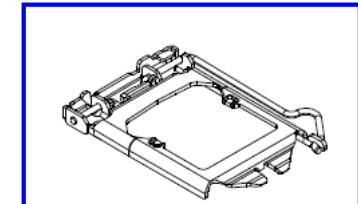




NOTE:

Lynnfield	ES2	QS	Production
HR27	NI	I	I
HR80	NI	I	I

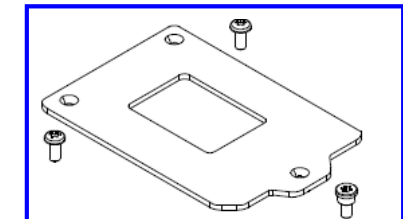
ILM1



INTEL LGA1156 SOCKET ILM

SOCKET1156_ILM

BACKPLATE1



INTEL LGA 1156P BACK PLATE, 3 SCREW

P144P11-6401

PEGATRON DT-MB RESTRICTED SECRET

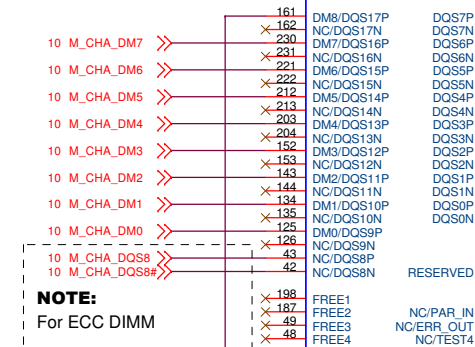
PEGATRON Title : CPU 1160 + MEMORY - 6

Pegatron Corp. Engineer: Vic_Chen

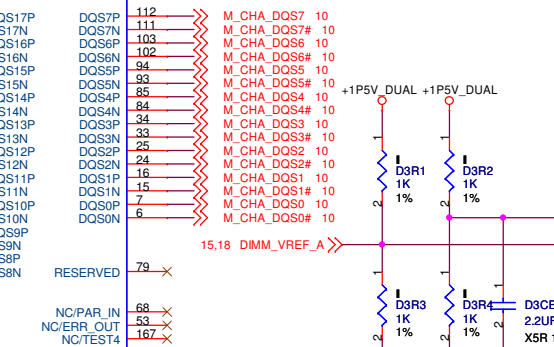
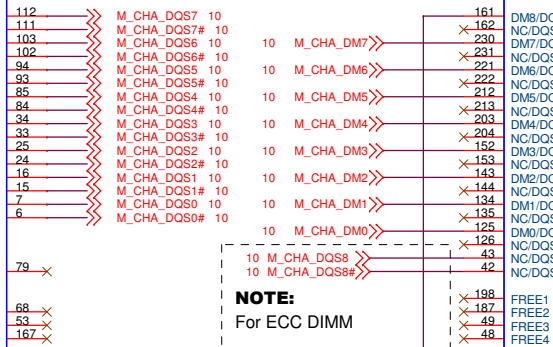
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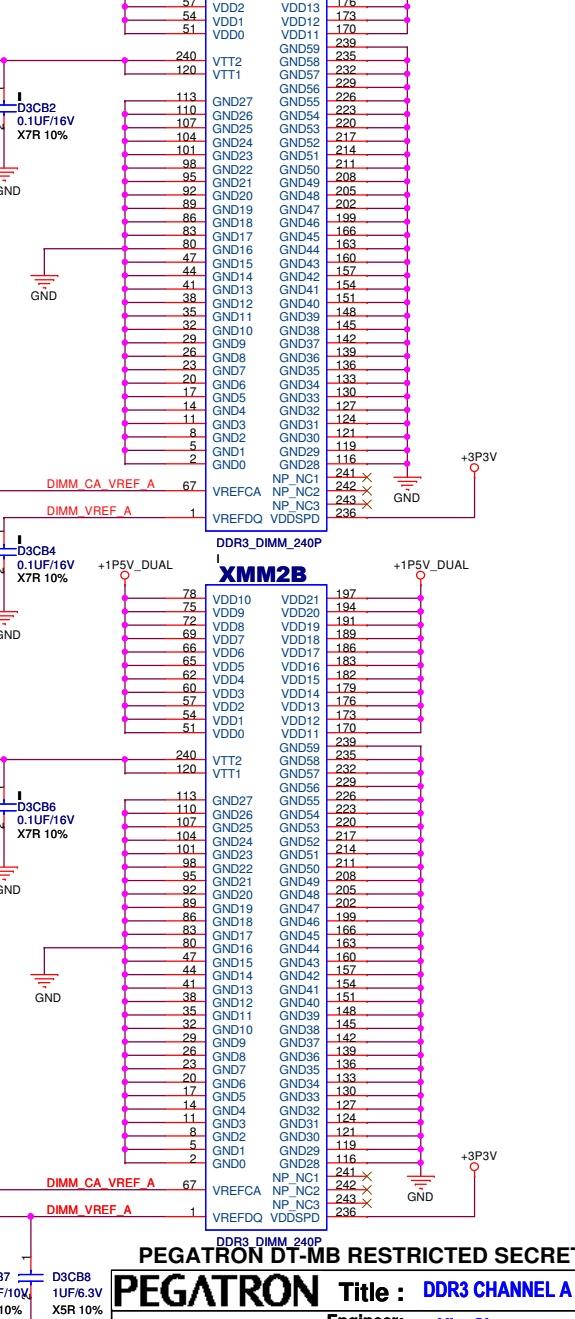
NOTE:
Check clock source if CPU implemented



—



DIMM_240P



GND

NOTE:
Check clock source if CPU
implemented

11 M_CHB_CLK1#
11 M_CHB_CLK0#
11 M_CHB_CLK0#

11 M_CHB_CS#1
11 M_CHB_CS#0
11 M_CHB_CKE1
11 M_CHB_CKE0
11 M_CHB_BA2
11 M_CHB_BA1
11 M_CHB_BA0

8,16,49,57 SMB DATA_M
8,16,49,57 SMB CLK_M
11 MB_ECC_CB[0..7]

NOTE:
For ECC DIMM

11 M_CHB_WE#
11 M_CHB_RAS#
11 M_CHB_CAS#
11 M_CHB_ODT1
11 M_CHB_ODT0

10,16 DDR3_DRAMRST#

11 M_CHB_DM7
11 M_CHB_DM6
11 M_CHB_DM5
11 M_CHB_DM4
11 M_CHB_DM3
11 M_CHB_DM2
11 M_CHB_DM1
11 M_CHB_DM0

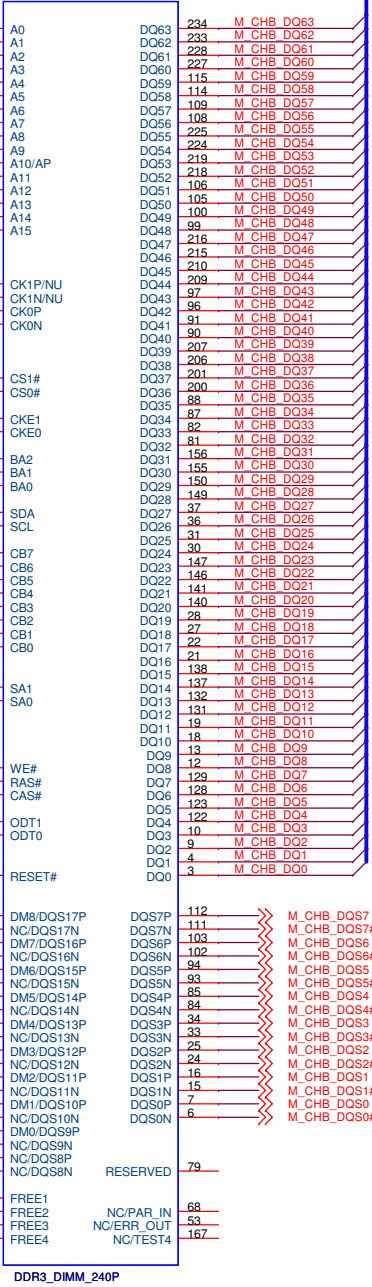
NOTE:
For ECC DIMM

11 M_CHB_DS8
11 M_CHB_DS8#

11 M_CHB_DS8#

XMM3 COLOR: BLUE

XMM3A



NOTE:
Check clock source if CPU
implemented

11 M_CHB_CLK3#
11 M_CHB_CLK2#
11 M_CHB_CLK2#

11 M_CHB_CS#3
11 M_CHB_CS#2
11 M_CHB_CKE3
11 M_CHB_CKE2
11 M_CHB_BA2
11 M_CHB_BA1
11 M_CHB_BA0

8,16,49,57 SMB DATA_M
8,16,49,57 SMB CLK_M
11 MB_ECC_CB[0..7]

NOTE:
For ECC DIMM

11 M_CHB_WE#
11 M_CHB_RAS#
11 M_CHB_CAS#
11 M_CHB_ODT3
11 M_CHB_ODT2

10,16 DDR3_DRAMRST#

11 M_CHB_DM7
11 M_CHB_DM6
11 M_CHB_DM5
11 M_CHB_DM4
11 M_CHB_DM3
11 M_CHB_DM2
11 M_CHB_DM1
11 M_CHB_DM0

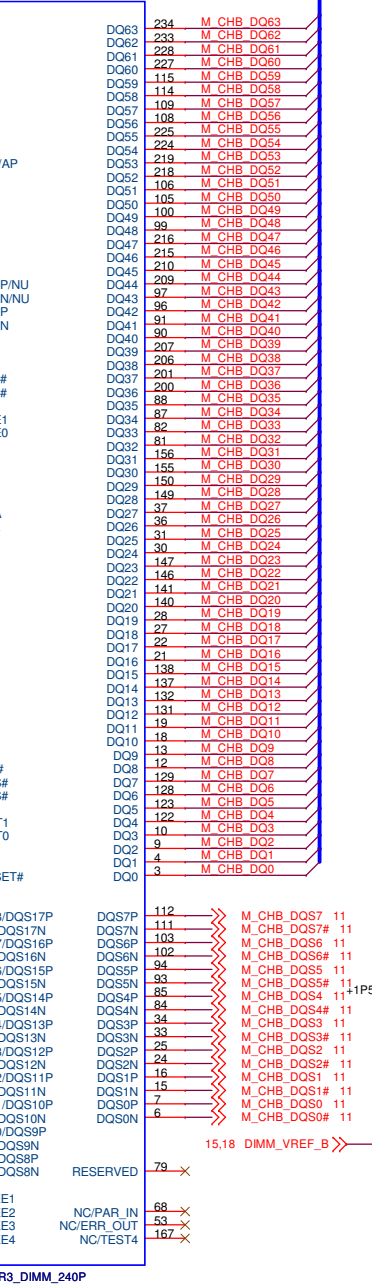
NOTE:
For ECC DIMM

11 M_CHB_DS8
11 M_CHB_DS8#

11 M_CHB_DS8#

XMM4 COLOR: BLACK

XMM4A



+SM_VTT

D3CB9
4.7UF/6.3V
X5R 10%
mx_c0805

D3CB10
0.1UF/16V
X7R 10%

D3CB11
0.1UF/16V
X7R 10%

D3CB12
0.1UF/16V
X7R 10%

D3CB13
4.7UF/6.3V
X5R 10%
mx_c0805

D3CB14
0.1UF/16V
X7R 10%

D3CB15
2.2UF/10V
X5R 10%

D3CB16
1UF/6.3V
X5R 10%

D3CB17
1K 1%

D3CB18
1K 1%

D3CB19
1K 1%

D3CB20
1K 1%

D3CB21
1K 1%

D3CB22
1K 1%

D3CB23
1K 1%

D3CB24
1K 1%

D3CB25
1K 1%

D3CB26
1K 1%

D3CB27
1K 1%

D3CB28
1K 1%

D3CB29
1K 1%

D3CB30
1K 1%

D3CB31
1K 1%

D3CB32
1K 1%

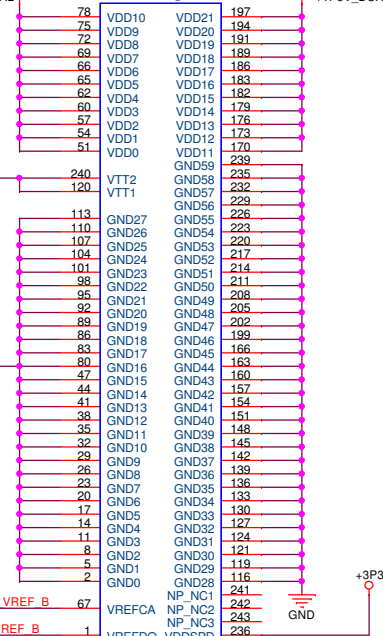
D3CB33
1K 1%

D3CB34
1K 1%

D3CB35
1K 1%

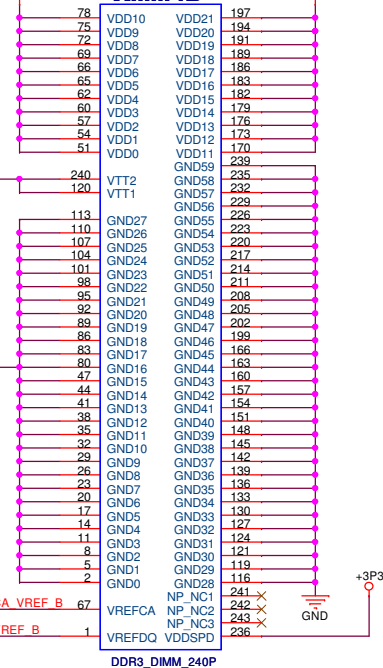
D3CB36
1K 1%

XMM3B



DDR3_DIMM_240P

XMM4B



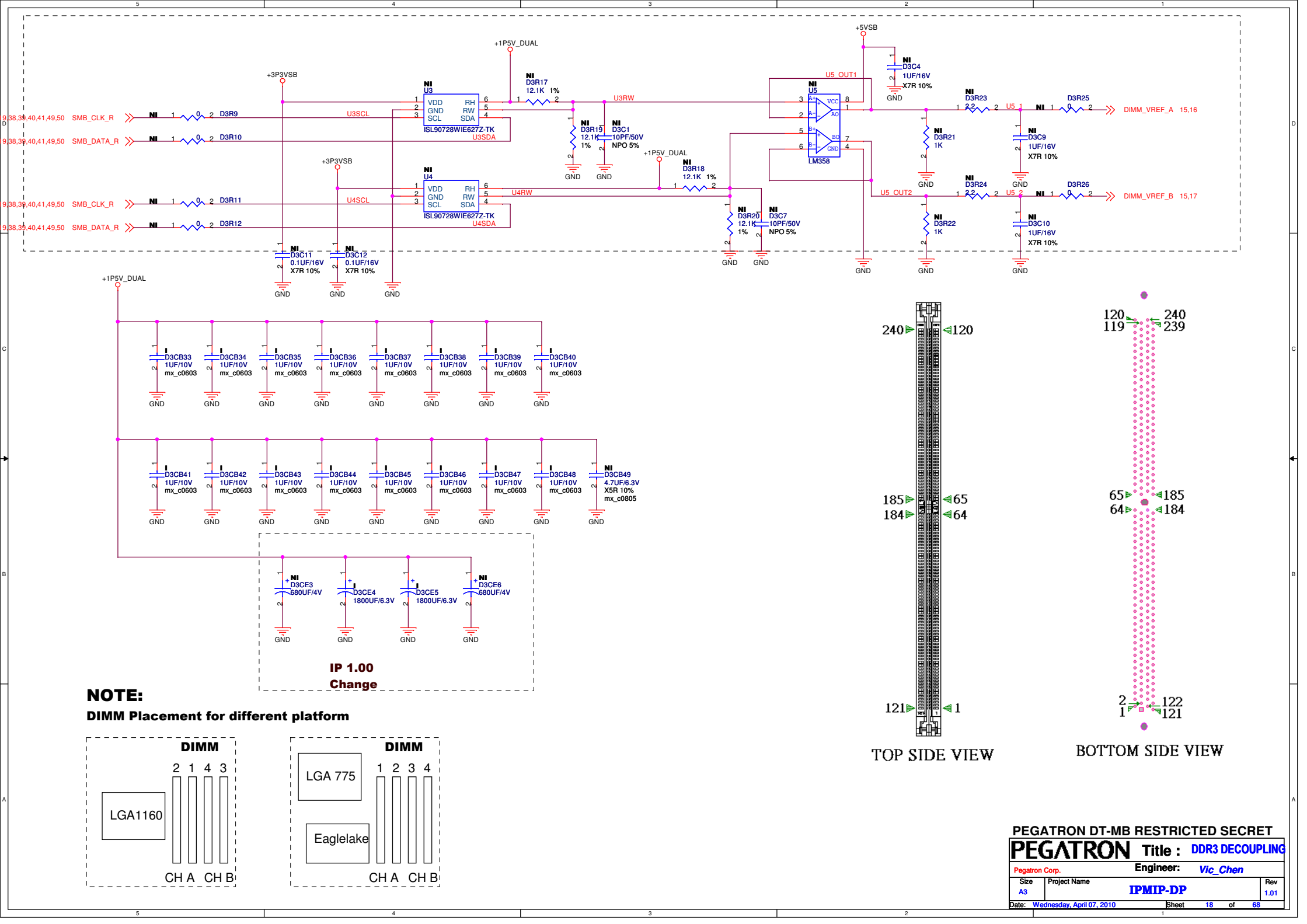
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title: DDR3 CHANNEL B

Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 17 of 68



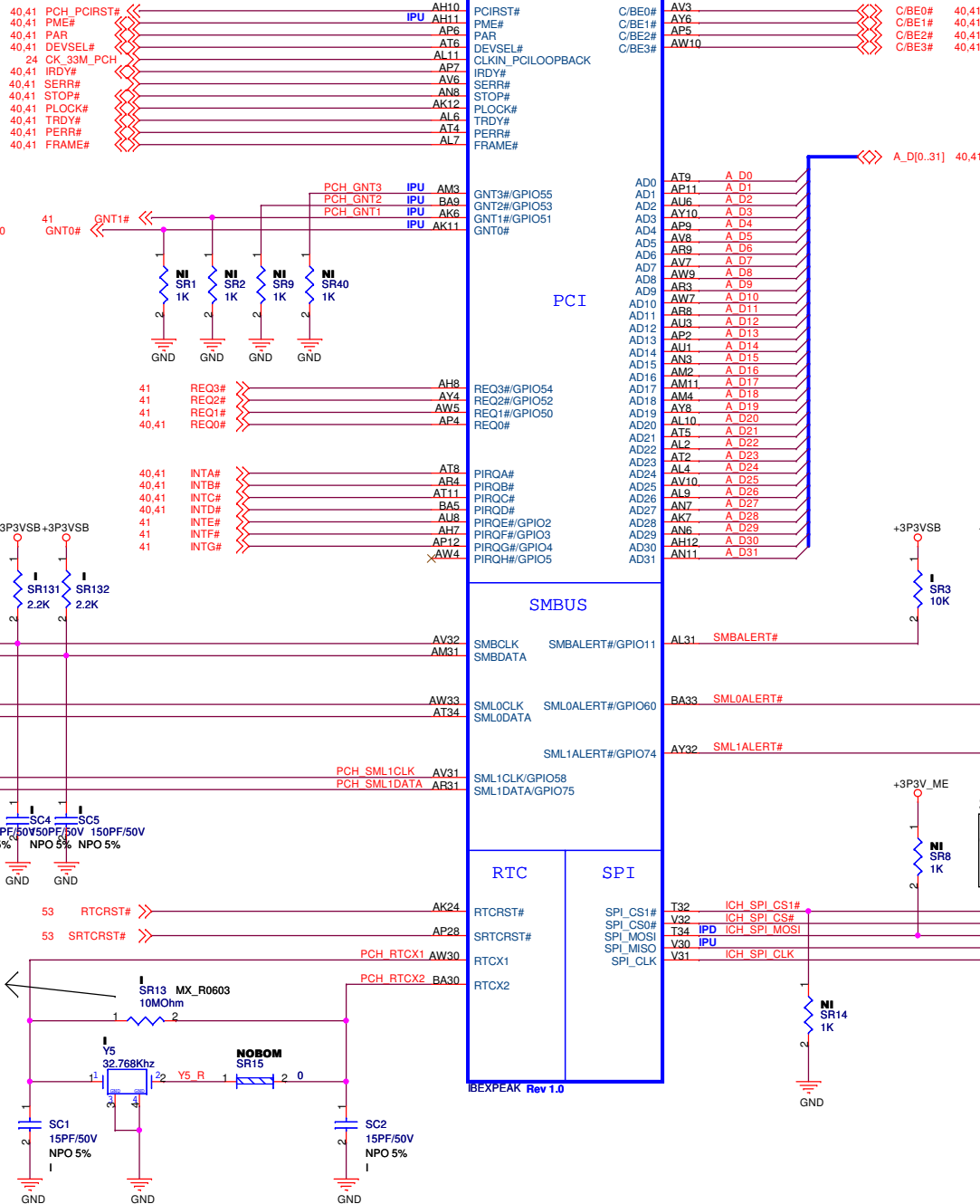
Strap

(GNT0#~GNT3# have IPU)

GNT3#	0	TOP Block SWAP
GNT3#	1	Normal (Default)

GNT2#	0	ESI mode (Server Only)
GNT2#	1	DMI (Default)

GNT1#	GNT0#	BOOT BIOS
1	0	RESERVED
0	1	PCI
1	1	SPI
0	0	LPC



Strap

SPI_MOSI (IPD)	0	Disable ITPM (Default)
SPI_MOSI (IPD)	1	Enable ITPM

CRB R1.0 (page.39) suggests that don't change it to 0402 package type



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 1

Pegatron Corp.

Engineer: Vic_Chen

Size A3 Project Name

IPMIP-DP

Rev 1.01

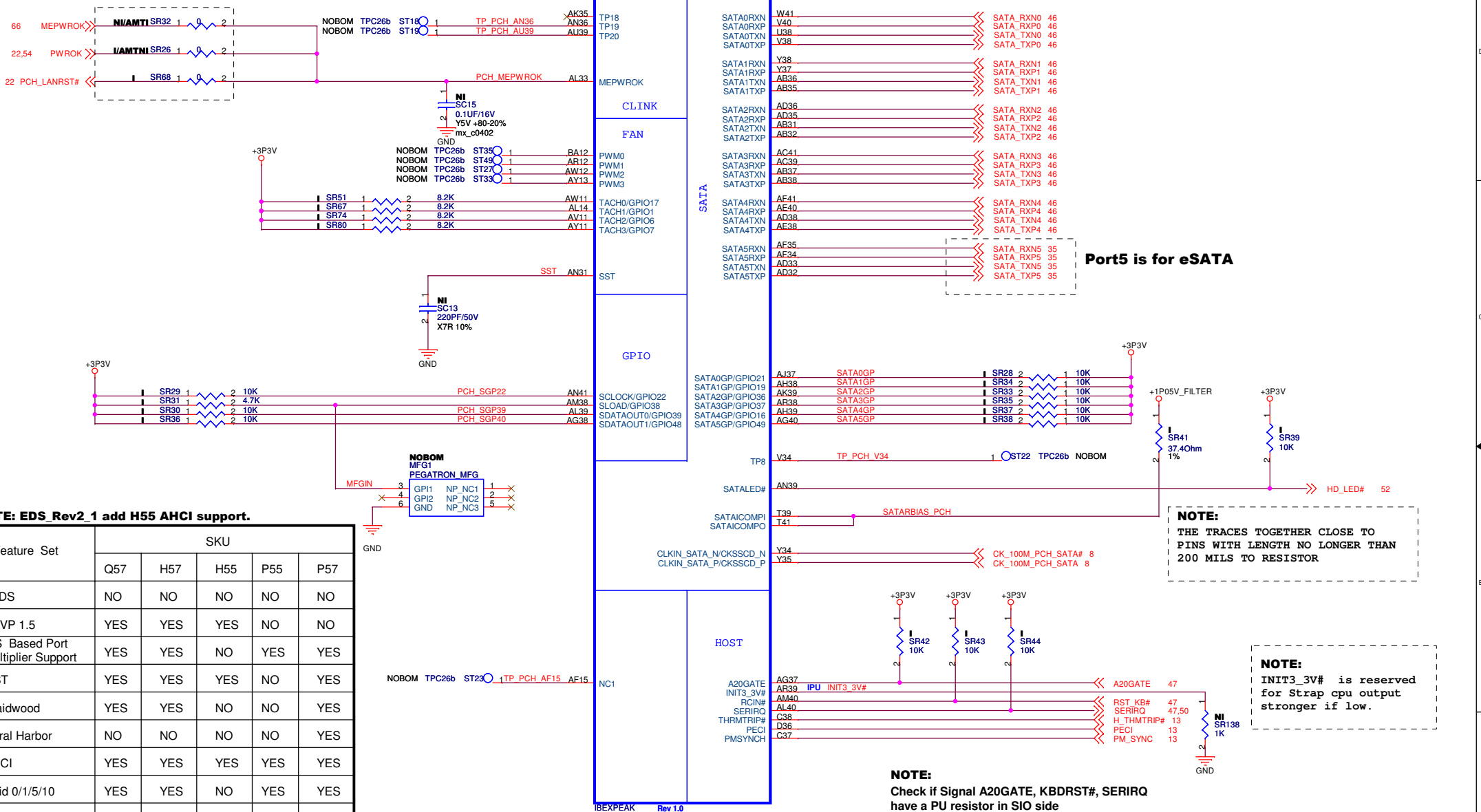
Date: Thursday, April 08, 2010

Sheet 19 of 68

NOTE:

Install SR32, SR68, NI SR26 if M3 support

Install SR26, SR68, NI SR32 if no M3 support



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 3

Pegatron Corp.

Engineer: Vic_Chen

Size A3 Project Name

IPMIP-DP

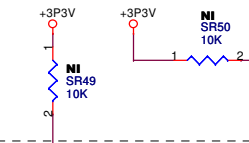
Rev

1.01

Date: Wednesday, April 07, 2010

Sheet 21 of 68

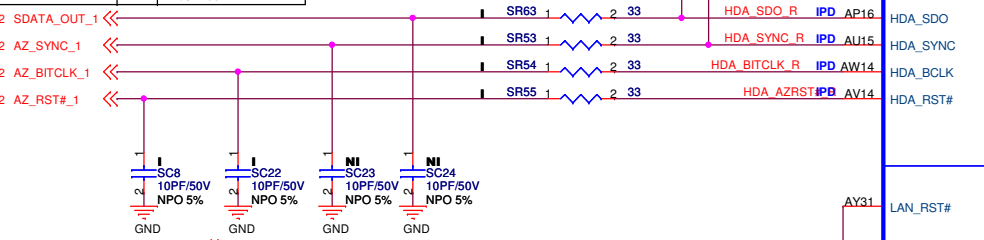
NOTE:
Internal Pull-up in PCH



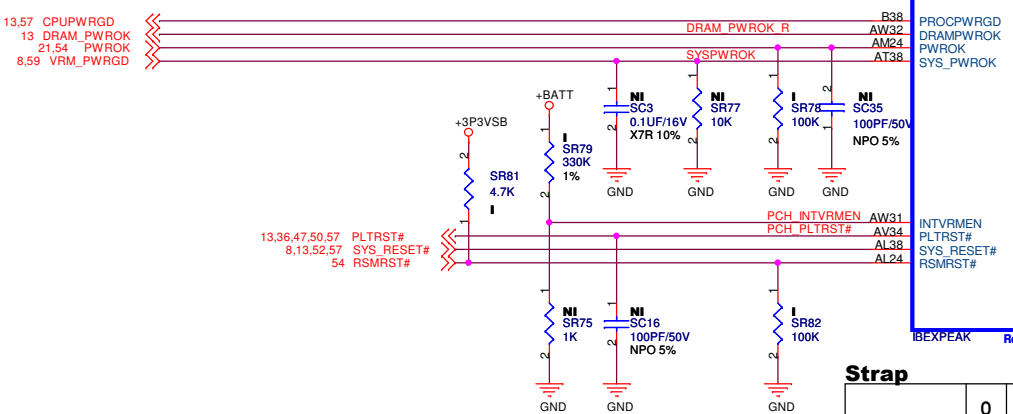
Strap

AZ_DATA_OUT (IPD)	0	1
0	USING CORE POWER FOR NAND FLASH	USING EPW POWER FOR NAND FLASH

AZ_SYNC (IPD)	0	1
0	OnDie PLL VR USE 1.8V SUPPLY	OnDie PLL VR USE 1.5V SUPPLY



NOTE:
Install for non-Intel LAN support



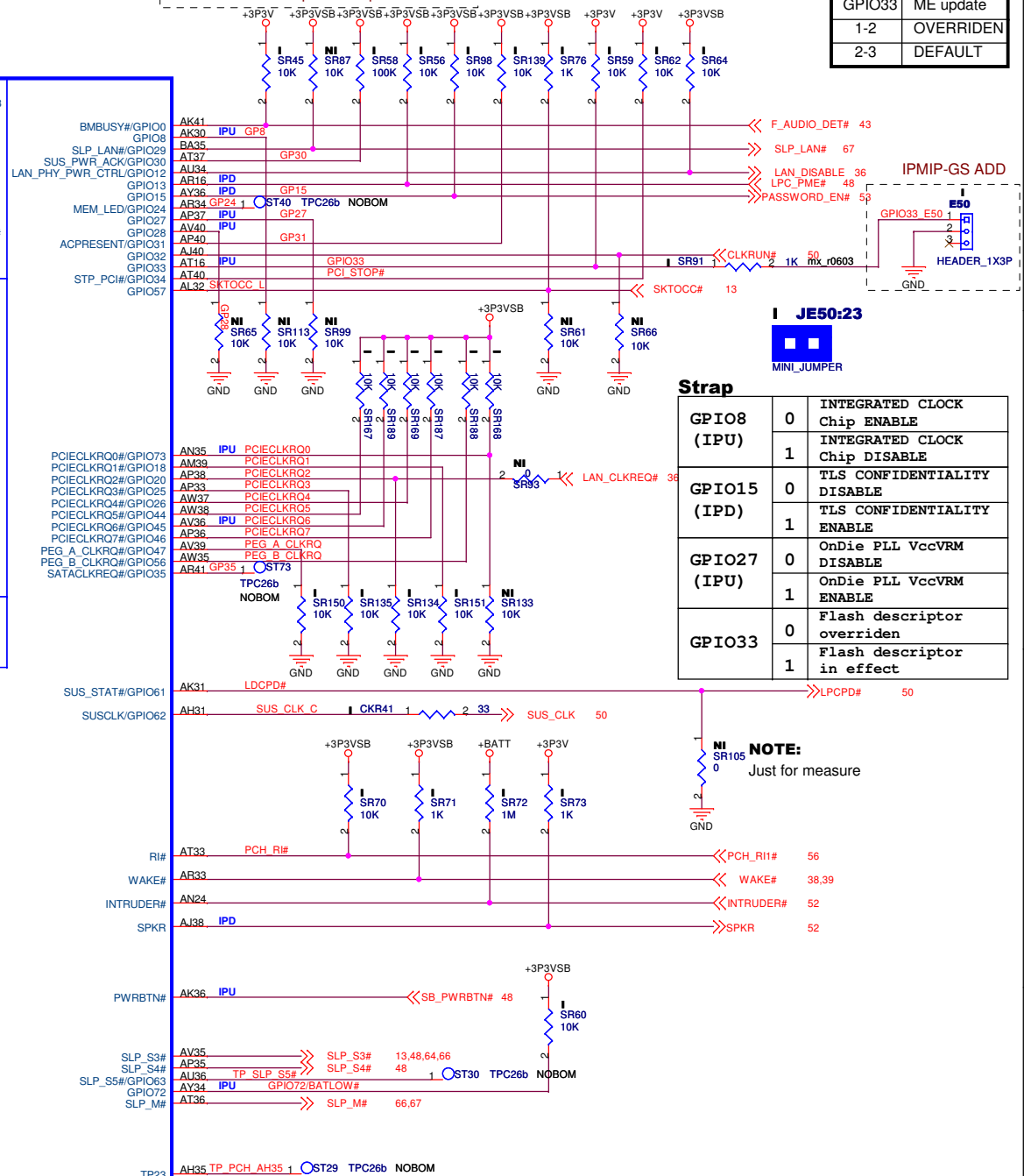
Strap

INTVRMEN	0	1
0	Disable intergrated 1.05V VRM for GbE	Enable (Default)

Strap

SPKR (IPD)	0	1
0	Disable No-reboot option	Enable No-reboot option

SR87 NI for power sequence t237



GPIO33	ME update
1-2	OVERRIDE
2-3	DEFAULT

Strap

GPIO8 (IPU)	0	1
0	INTEGRATED CLOCK Chip ENABLE	INTEGRATED CLOCK Chip DISABLE
GPIO15 (IPD)	0	1
0	TLS CONFIDENTIALITY DISABLE	TLS CONFIDENTIALITY ENABLE
GPIO27 (IPU)	0	1
0	OnDie PLL VccVRM DISABLE	OnDie PLL VccVRM ENABLE
GPIO33	0	1
0	Flash descriptor overridden	Flash descriptor in effect

NOTE:
Just for measure

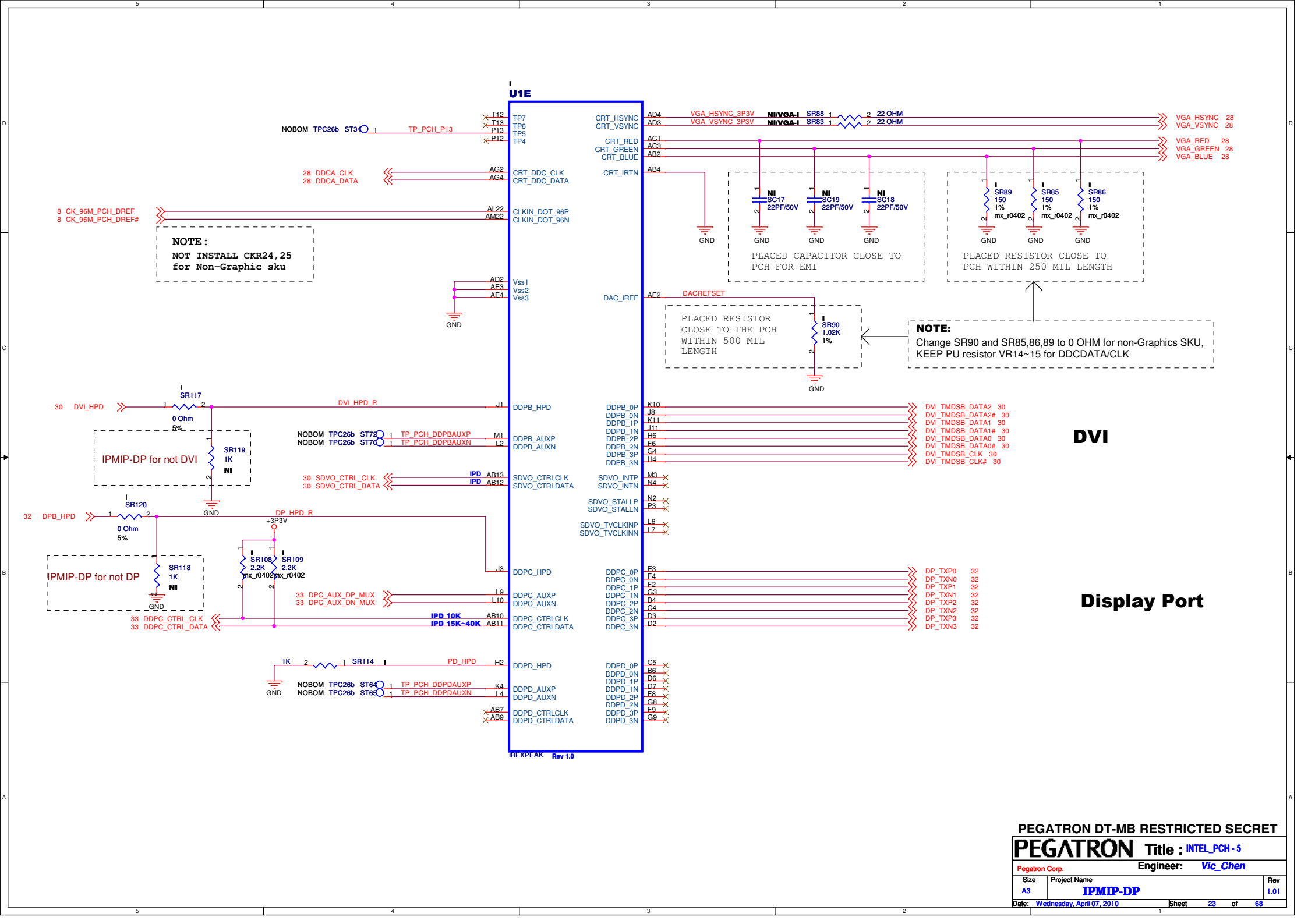
PEGATRON DT-MB RESTRICTED SECRET

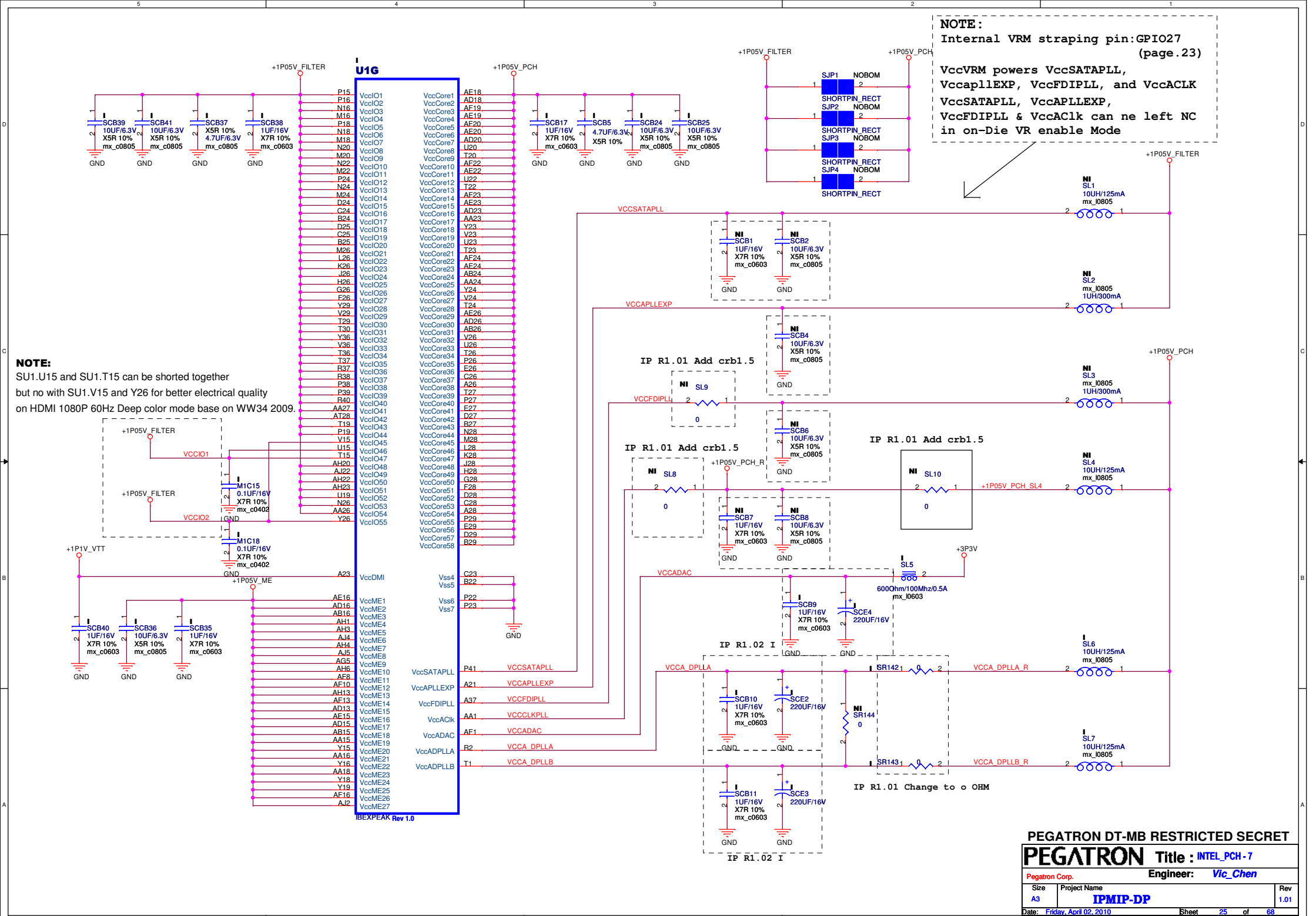
PEGATRON Title : INTEL_PCH - 4

Pegatron Corp. Engineer: Vic_Chen

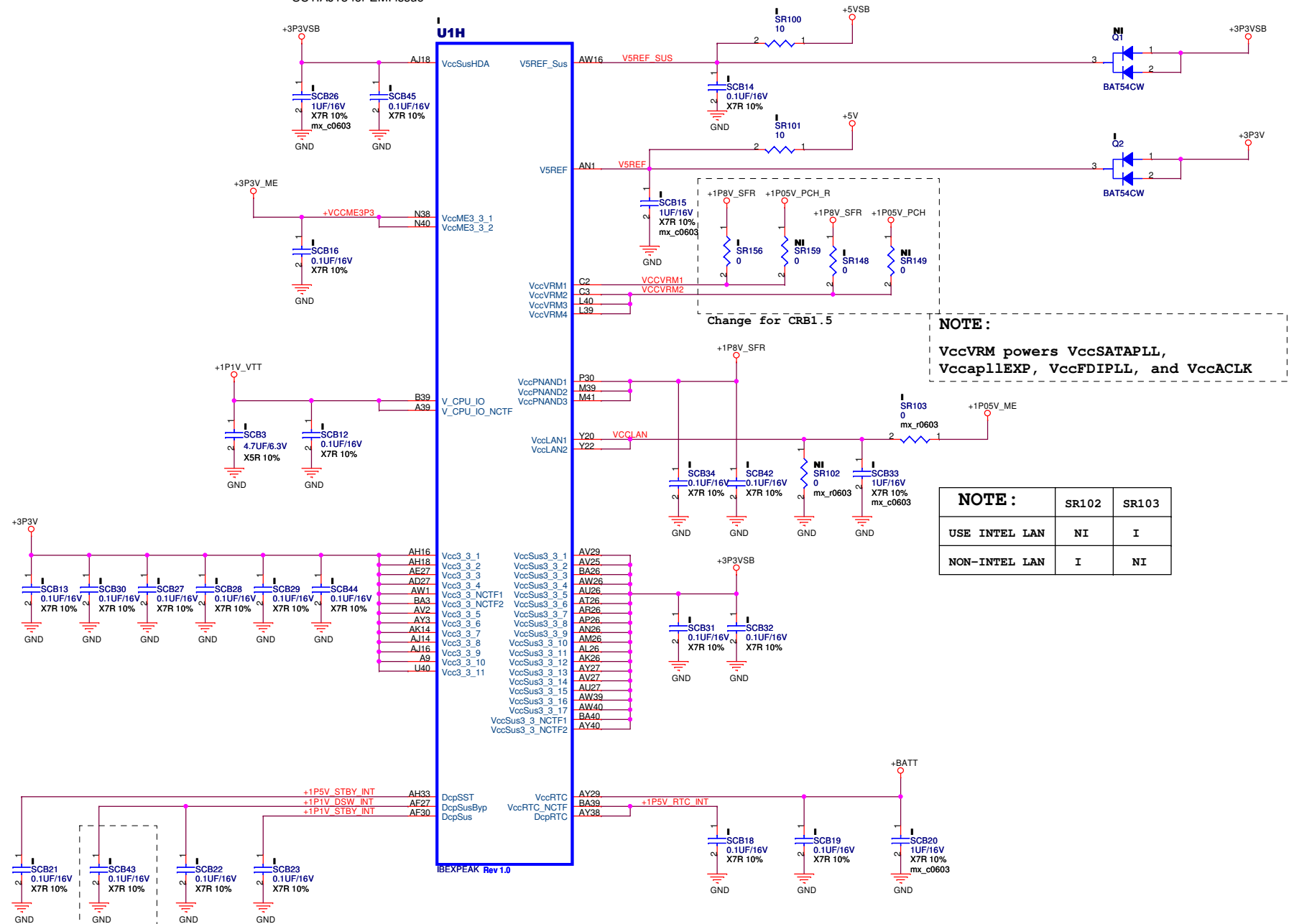
Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 22 of 68





Note
Place SCB45 close to
SU1.AJ18 for EMI issue



NOTE:
MOW WW08 recommand to reserved SCB43.

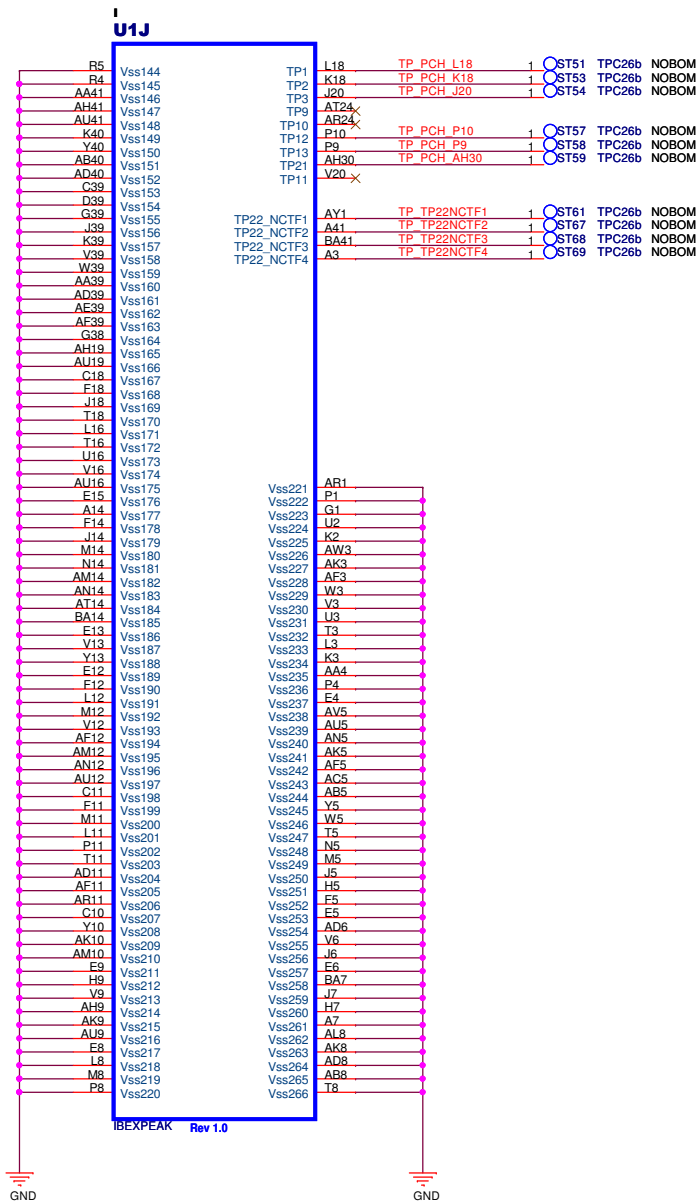
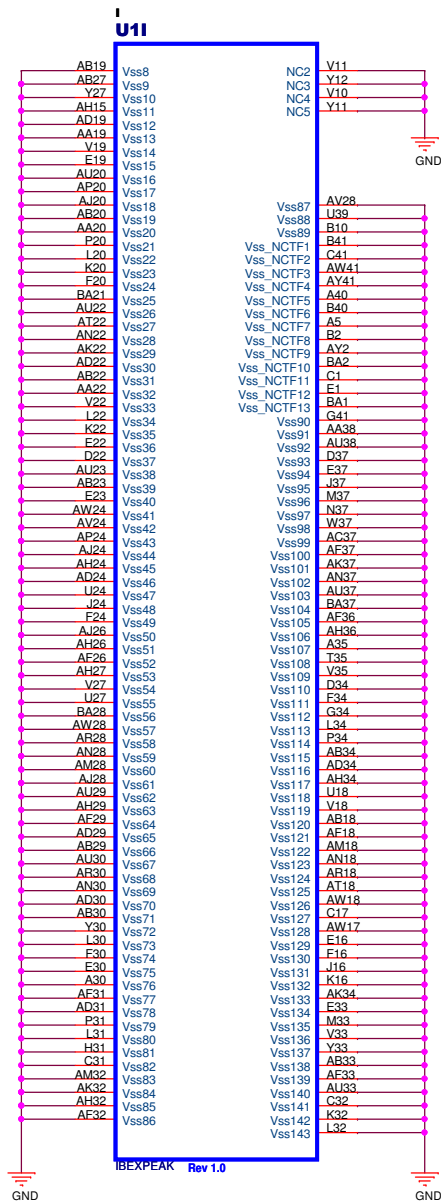
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 8

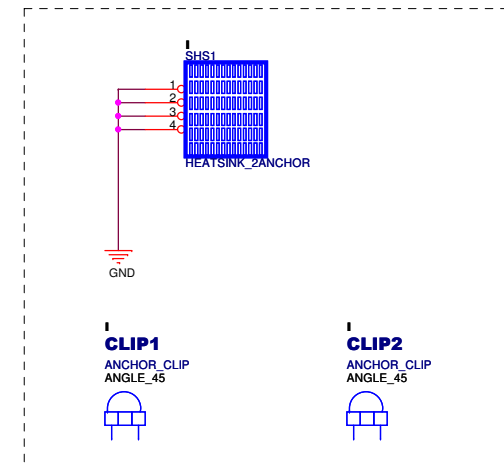
Pegatron Corp. **Engineer:** *Vic_Chen*

Size A3	Project Name IPMIP-DP	Rev 1.01
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Date: Tuesday, March 23, 2010 Sheet 26 of 68

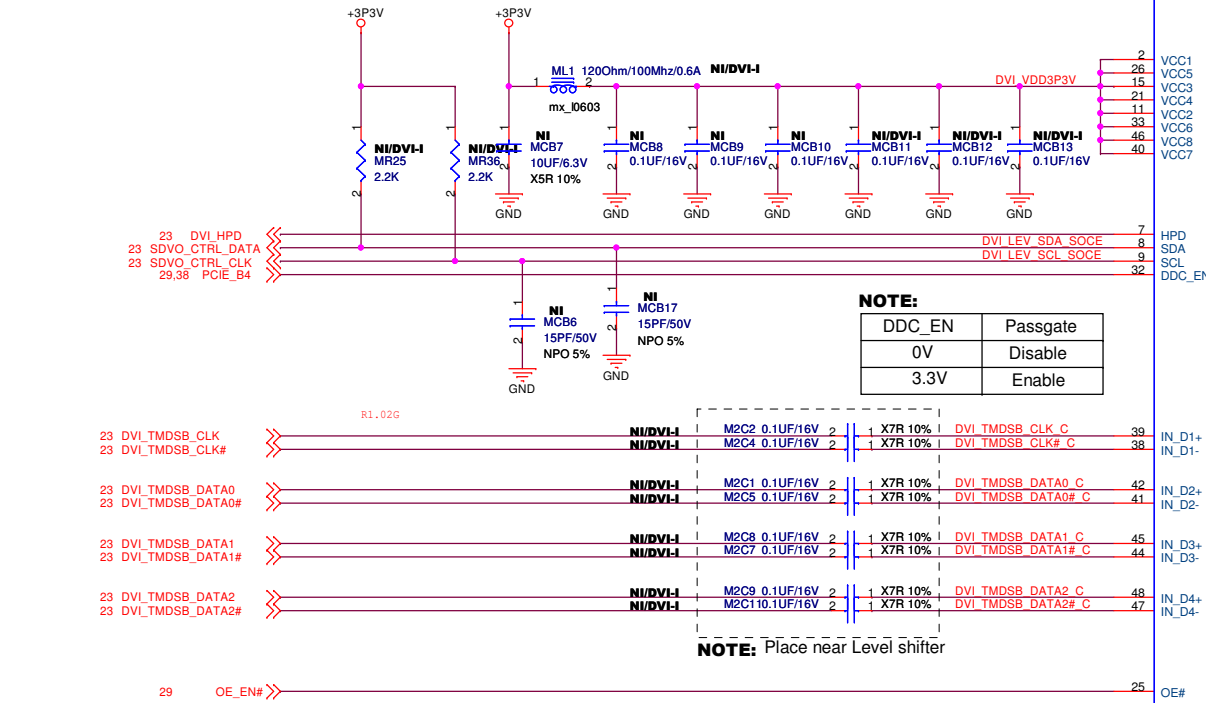


NOTE:
BOM option depend on thermal result



CH7318: 02G480001000
ASM1442: 022U-0004000

MU5



NOTE: Pericom PI3VDP411LS

Pin 3, 4, 6, 10, 34, and 35 are internal 100K ohm pull-up

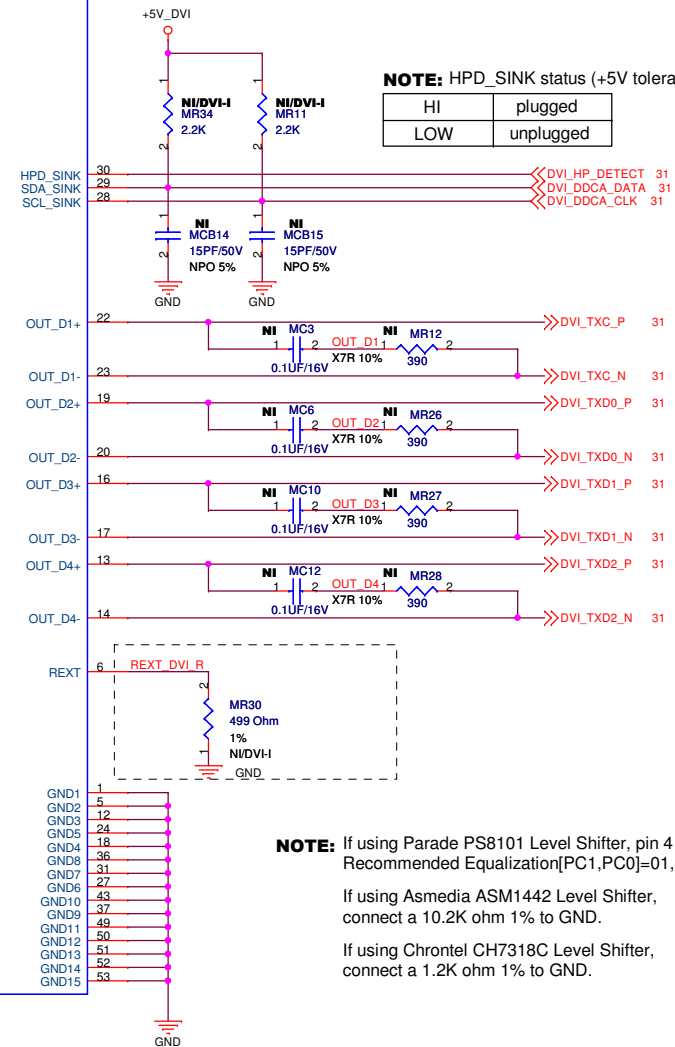
OC_3 (Pin10)	OC_2 (Pin6)	OC_1 (Pin4)	OC_0 (Pin3)	Vswing (mV)	Pre/Deemphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

NOTE: Pericom PI3VDP411LS

EQ0 (Pin34)	EQ1 (Pin35)	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

NOTE:

OE*	IN_D Termination	OUT_D Outputs
1	Hi-Z	Hi-Z
0	50ohm	Active



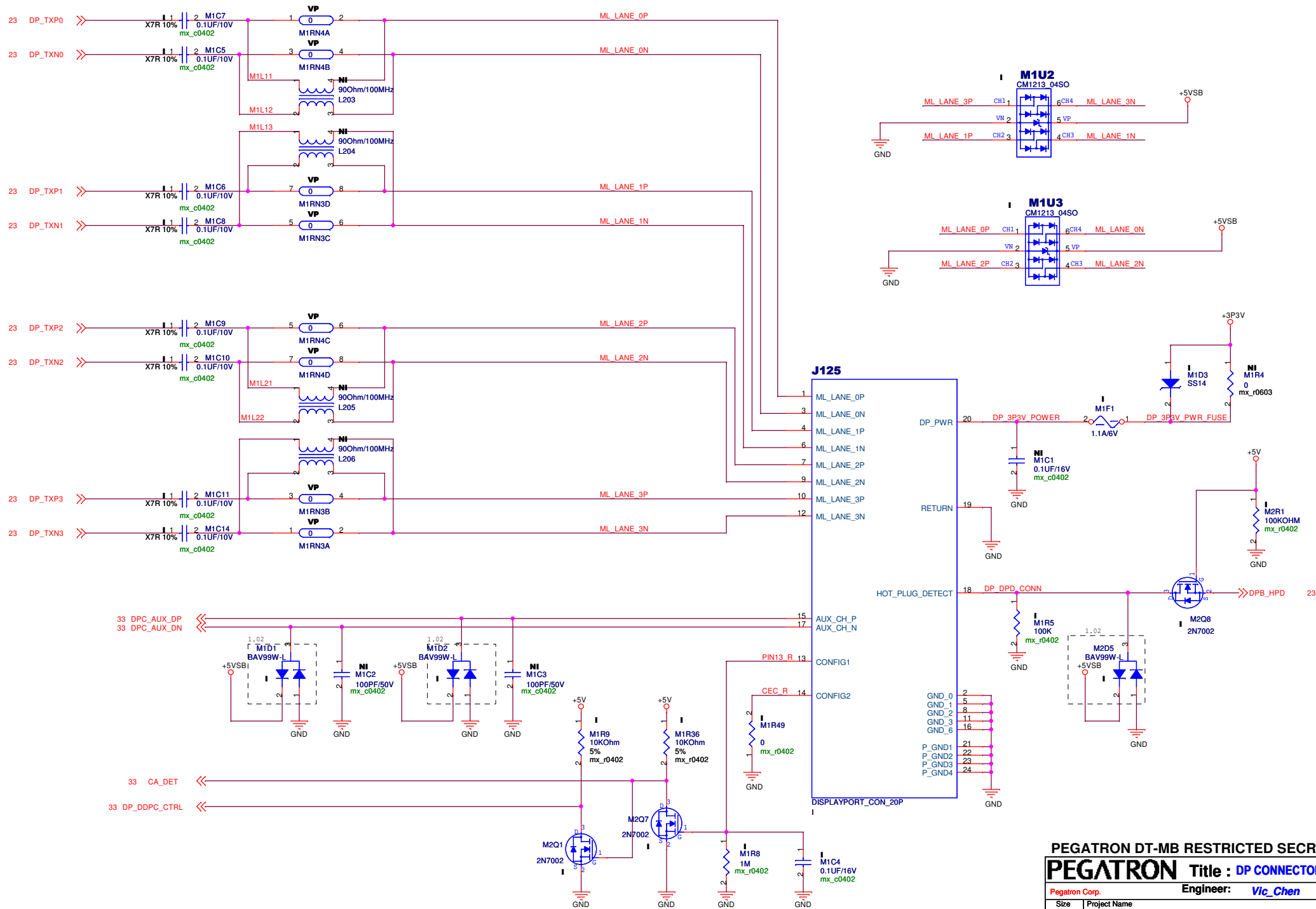
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DVI Level shifter

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 30 of 68



PEGATRON DT-MB RESTRICTED SECRET

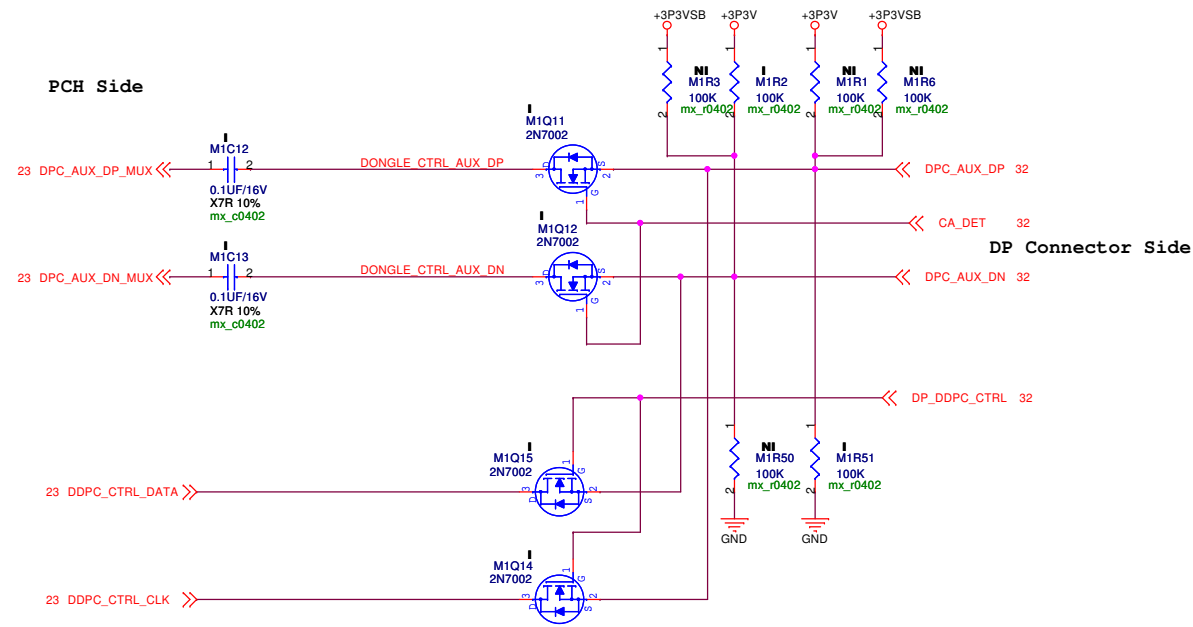
PEGATRON Title : DP CONNECTOR

Pegatron Corp. Engineer: Vic Chen

Size A3 Project Name IPMP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 32 of 68

Display Port to HDMI/DVI Dongle control



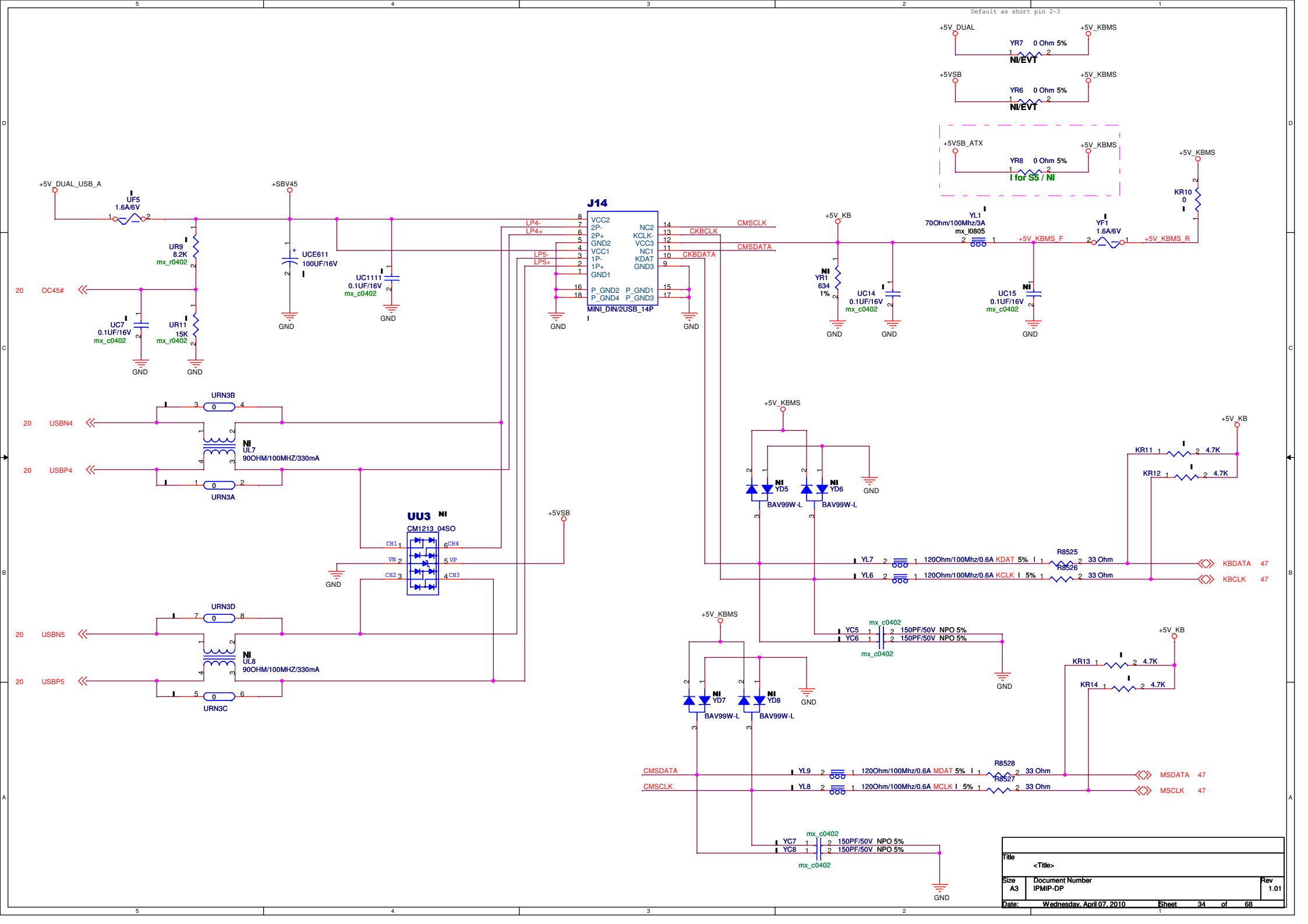
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DP DONGLE

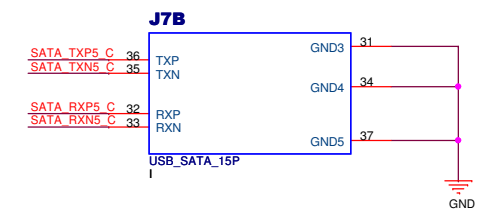
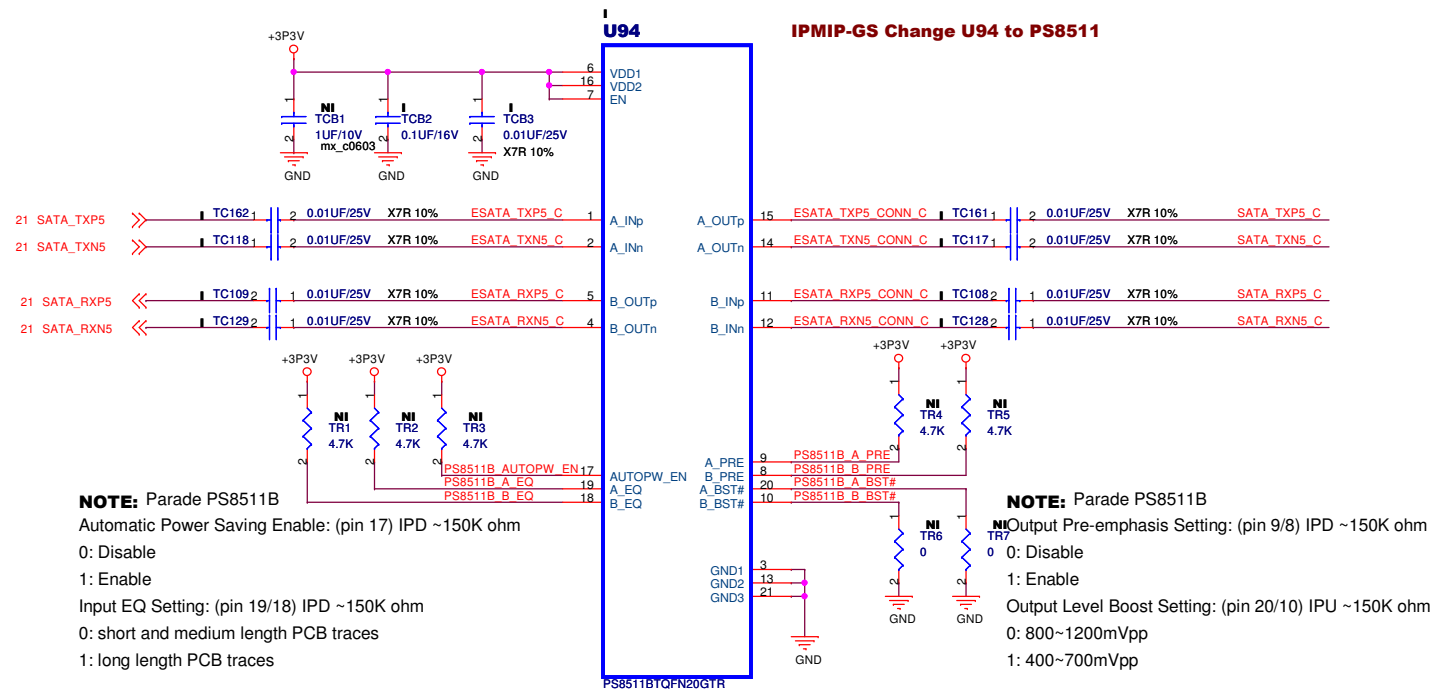
Pegatron Corp. Engineer: Vic_Chen

Size A3	Project Name IPMIP-DP	Rev 1.01
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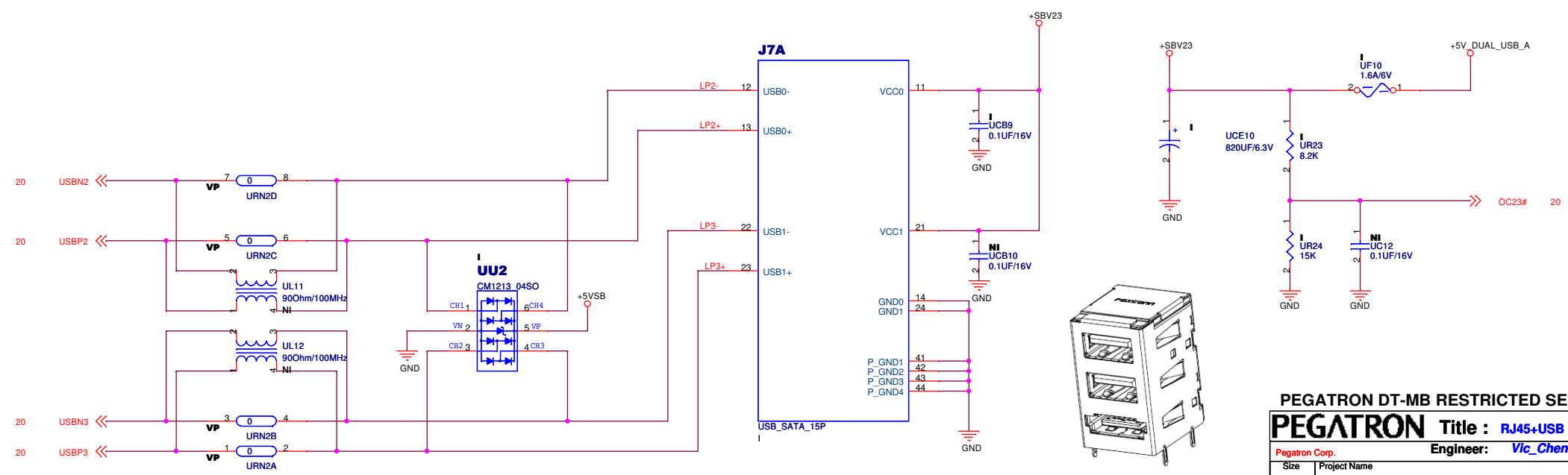
Date: Wednesday, April 07, 2010 Sheet 33 of 68

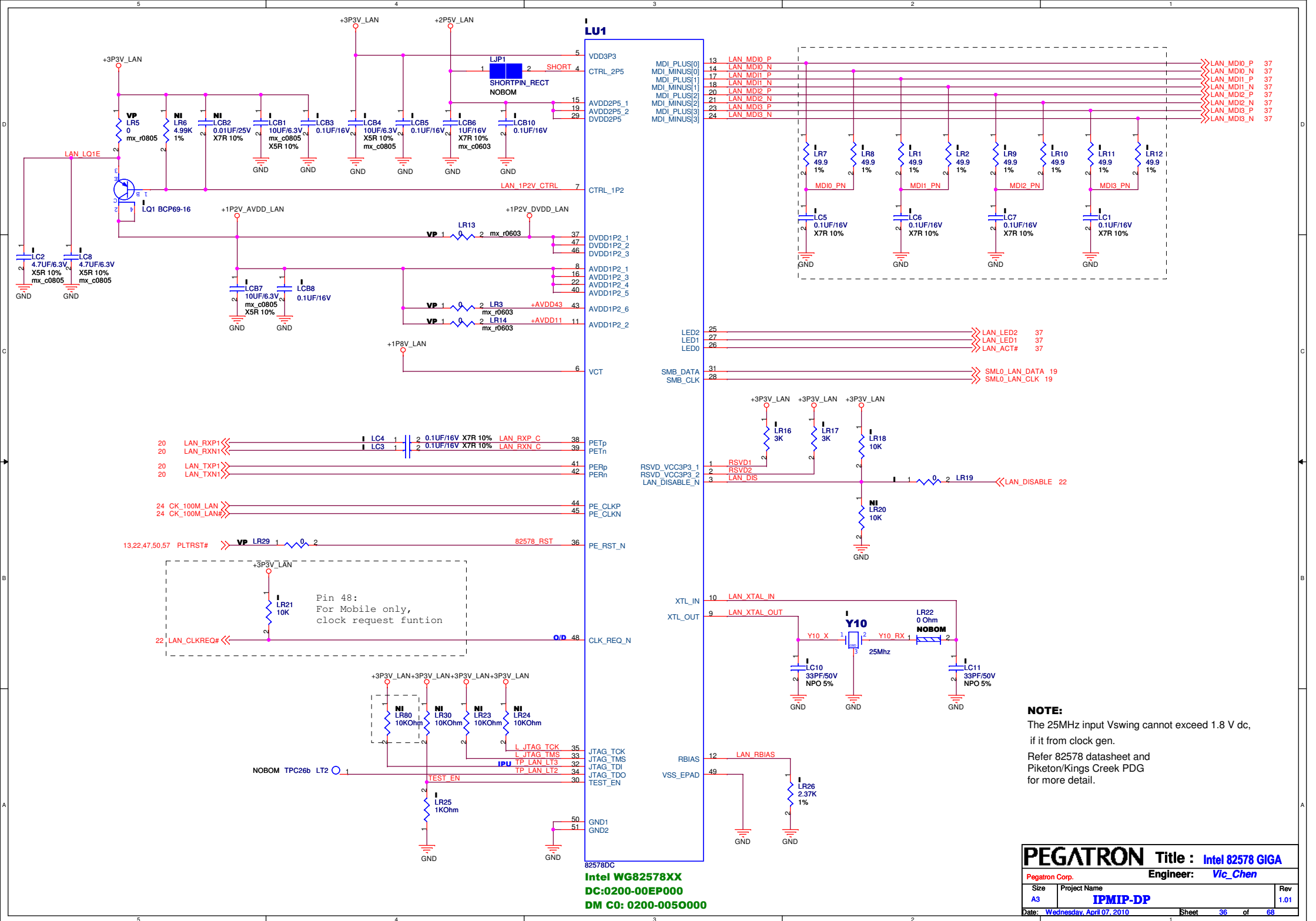


Title			<Title>
Size	A3	Document Number	IPMIP-DP
Date:	Wednesday, April 07, 2010	Sheet	34 of 68
Rev	1.01		



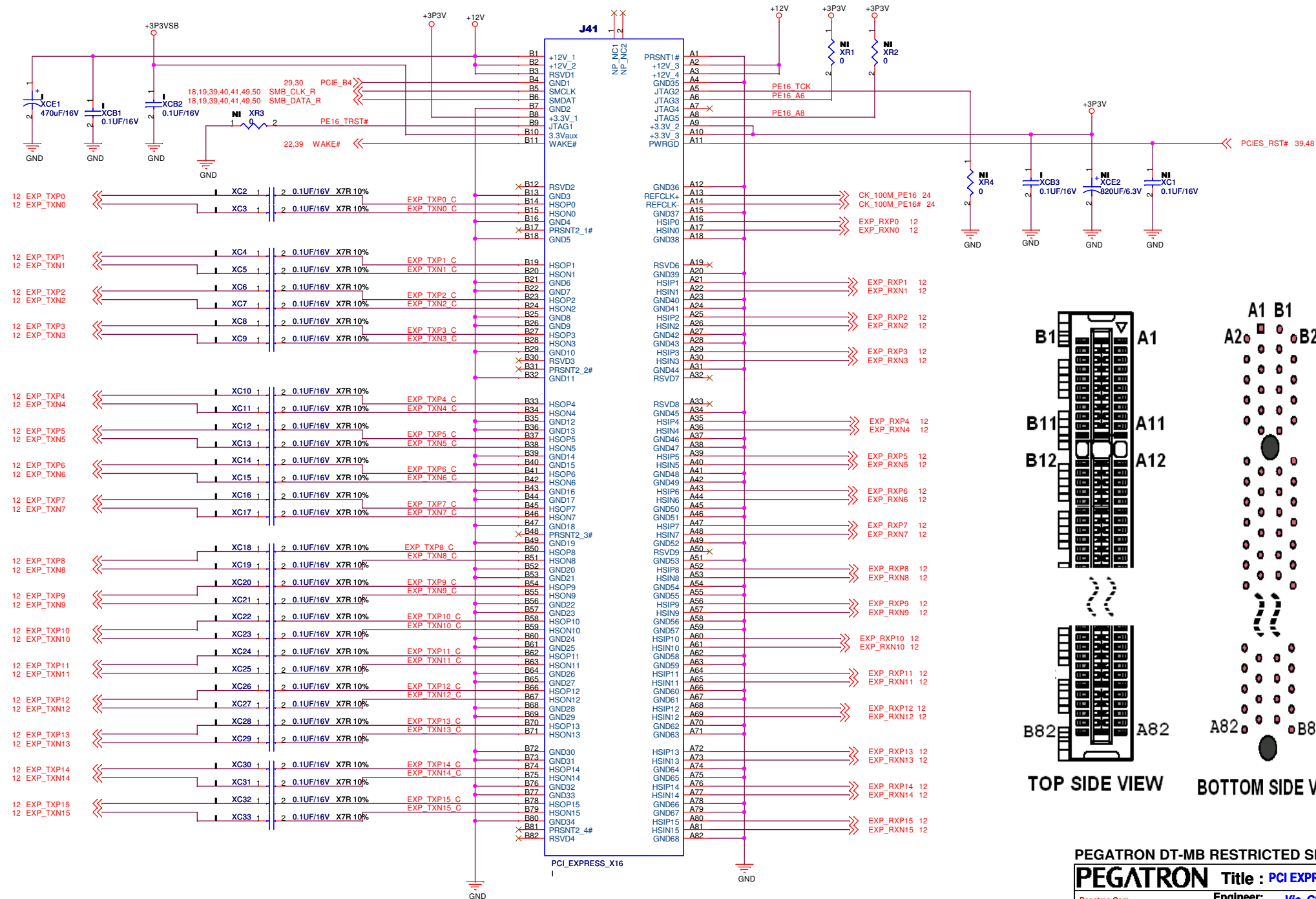
E-SATA + Dual USB CONNECTOR





Intel WG82578XX
DC:0200-00EP000
DM C0: 0200-0050000

PCI EXPRESS X16 Graphics Card Slot



PEGATRON DT-MB RESTRICTED SECRET

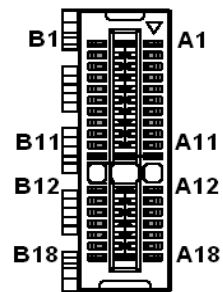
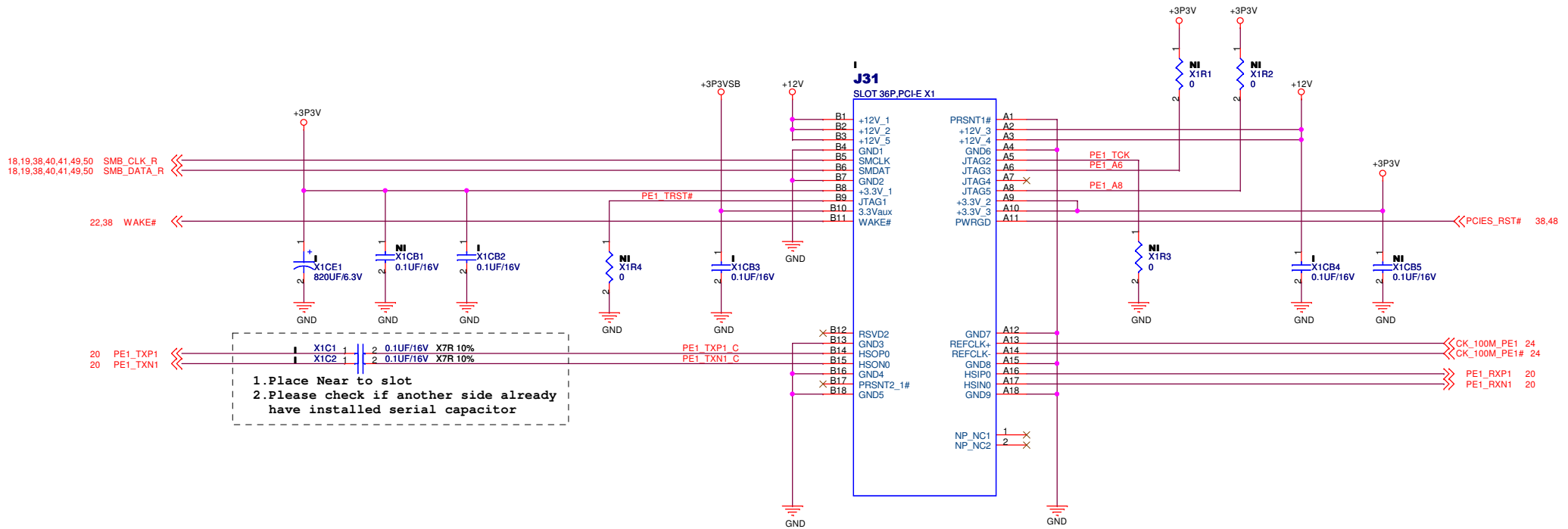
PEGATRON Title : PCI EXPRESS X16

Pegatron Corp. Engineer: **Vic Chen**

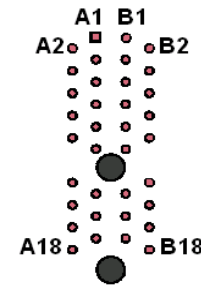
Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 38 of 68

PCI Express x1 SLOT



TOP SIDE VIEW



BOTTOM SIDE VIEW

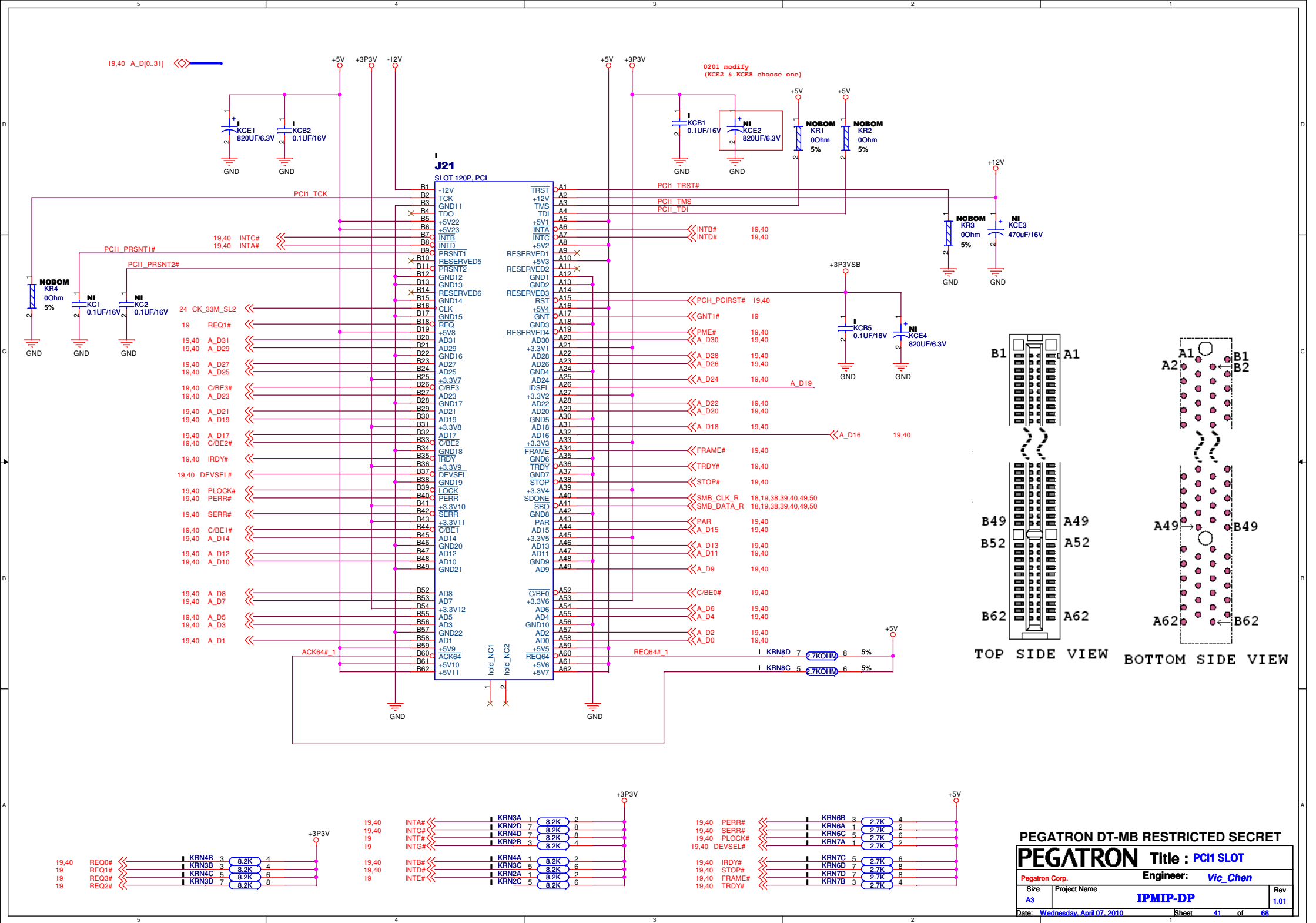
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **PCI EXPRESS X1**

Pegatron Corp. Engineer: **Vic_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

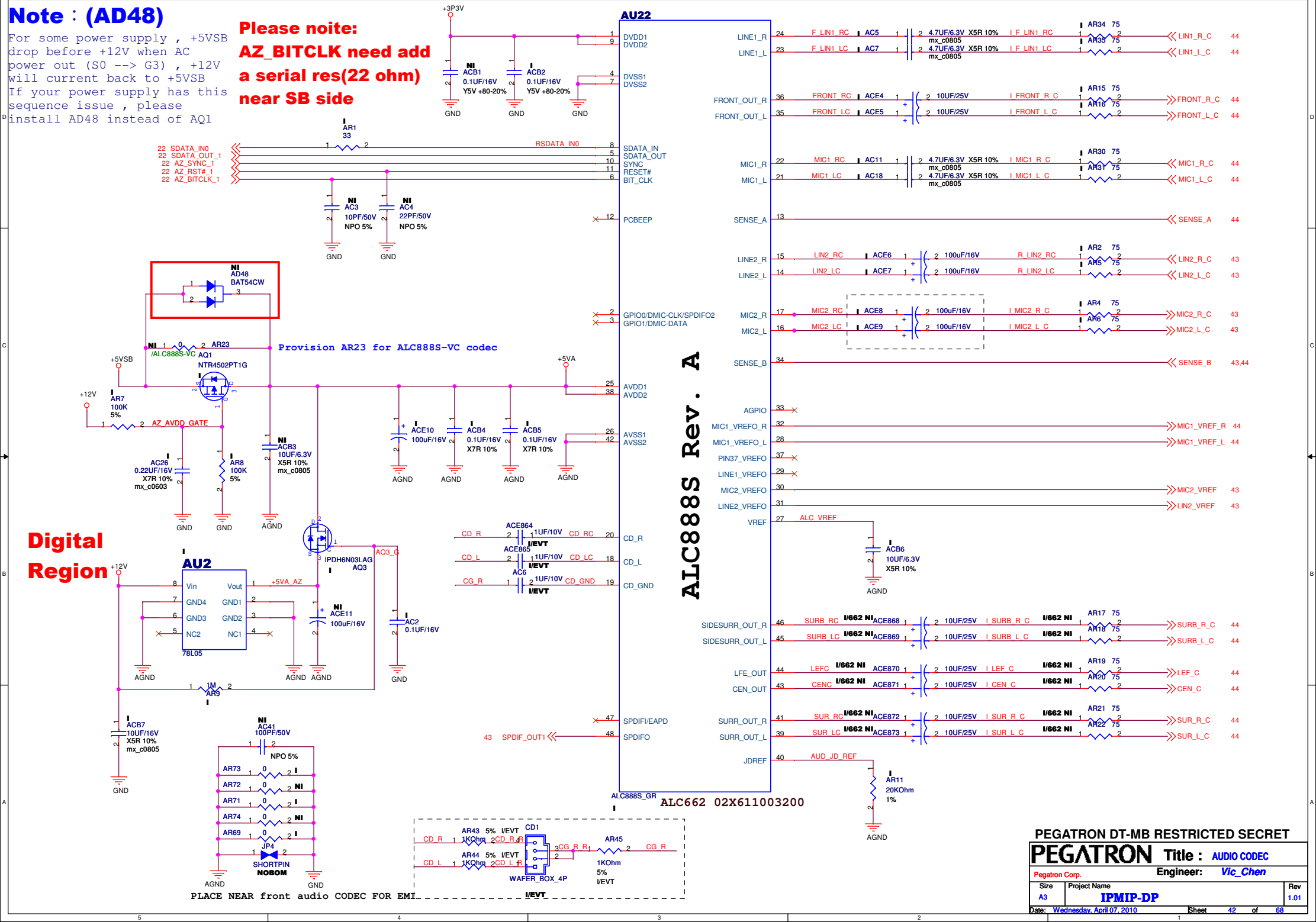
Date: Wednesday, April 07, 2010 Sheet 39 of 68

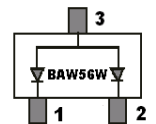


Note : (AD48)

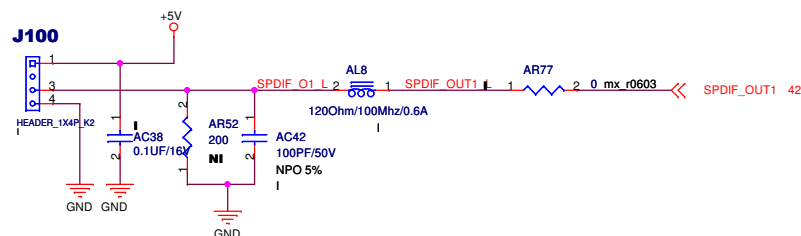
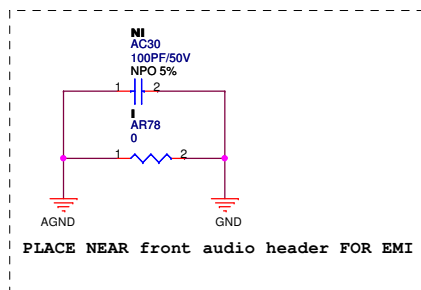
For some power supply , +5VSB drop before +12V when AC power out (S0 --> G3) , +12V will current back to +5VSB. If your power supply has this sequence issue , please install AD48 instead of AQ1

Please noite:
AZ_BITCLK need add a serial res(22 ohm) near SB side



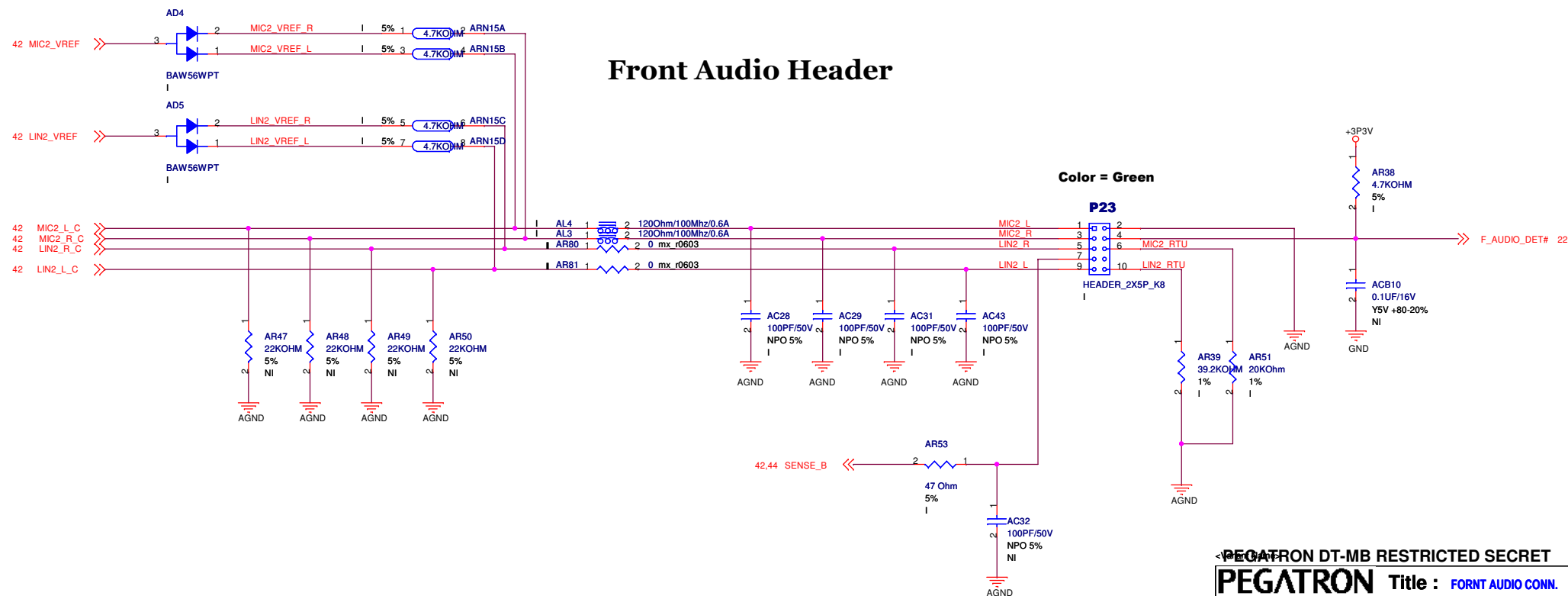


TOP SIDE VIEW



But for other customers (ex, Intel, EPSON, FSC, Dell.....etc), they might don't need 6+3 configuration, just general 6+2 type. If so, please change LINE1 (Pin 23/24) to Rear Line-In port instead of CD-IN, because CD-IN (Pin 18/19/20) port is only dedicated input port and can't retasking

Front Audio Header



<PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FORNT AUDIO CONN.

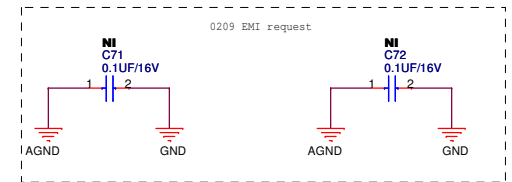
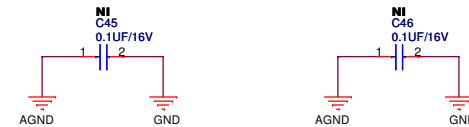
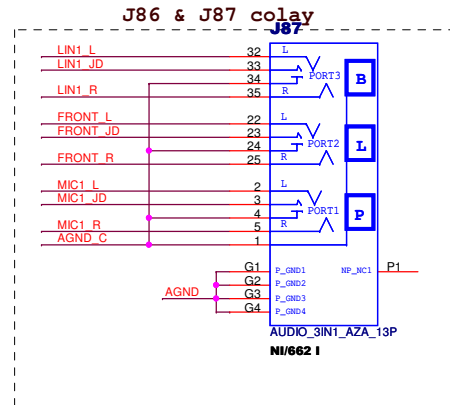
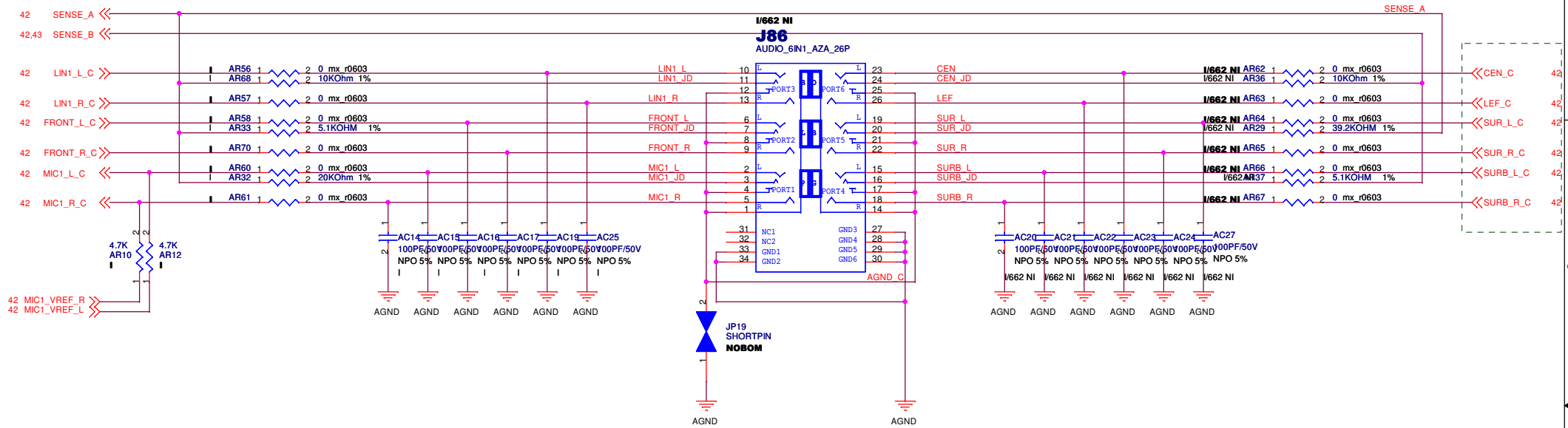
Pegatron Corp. Engineer: Vic Chen

Size A3 Project Name IPMP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 43 of 68

Azalia Rear Audio Connector

IPMIP-GS R1.01 Change port



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : REAR AUDIO CONN.

Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 44 of 68

Pin49:
System clock input: 24/48
MHz

Pin 39: SERIRQ
Please check if SB side already
have a pull-up resistor!

22.50 LAD0
22.50 LAD1
22.50 LAD2
22.50 LAD3
22.50 LFRAME#
22 LDRO#
24 CK_30M_SIO
21.50 SERIRQ
8 CK_48M_SIO

34 KBCLK
34 KBDATA
34 MSCLK
34 RST_KB#
21 A20GATE

56 DCD1#
56 RI1#
56 CTS1#
56 DTR1#
56 RTS1#
56 DSR1#
56 TXD1
56 RXD1

55 XSTB#
55 XAFD#
55 ERROR#
55 ACK#
55 BUSY
55 PE
55 SLCT
55 XPD0
55 XPD1
55 XPD2
55 XPD3
55 XPD4
55 XPD5
55 XPD6
55 XPD7
55 XSLIN#
55 XINIT#

41 LAD0
42 LAD1
43 LAD2
44 LAD3
40 LFRAME#
38 LDRO#
37 LRESET#
47 PCCLK
39 SERIRQ
49 CLKIN

80 KDAT/GP61
81 KCLK/GP60
82 MDAT/GP57
83 MCLK/GP56
46 KRST#/GP62
GA20/JP5

127 DCD1#
128 RI1#
126 CTS1#
122 DTR1#/JP4
123 RTS1#
124 DSR1#
125 SOUT1/JP3
SIN1

26 DCD2#
28 RI2#
27 CTS2#
29 DTR2#
23 RTS2#
22 DSR2#
21 TXD2
20 RXD2

26 DCD2#/GP21
28 RI2#/GP17
27 CTS2#/GP20
29 DTR2#
23 FAN_TACS/RTS2#/GP24
22 FAN_TACA/DSR2#/GP25
21 SOUT2/GP26
SIN2/GP27

IT8721F

AVCC3

3VSB1
3VSB2
3VSB3

VBAT

SYS_3VSB

+5VSB_ATX

+5VSB

5VSB_CTRL

GNDA

GNDD1

GNDD2

GNDD3

GNDD4

TSD

NOTE :

O2Q1 MOS Selection
Base on your platform
Please check Power guy

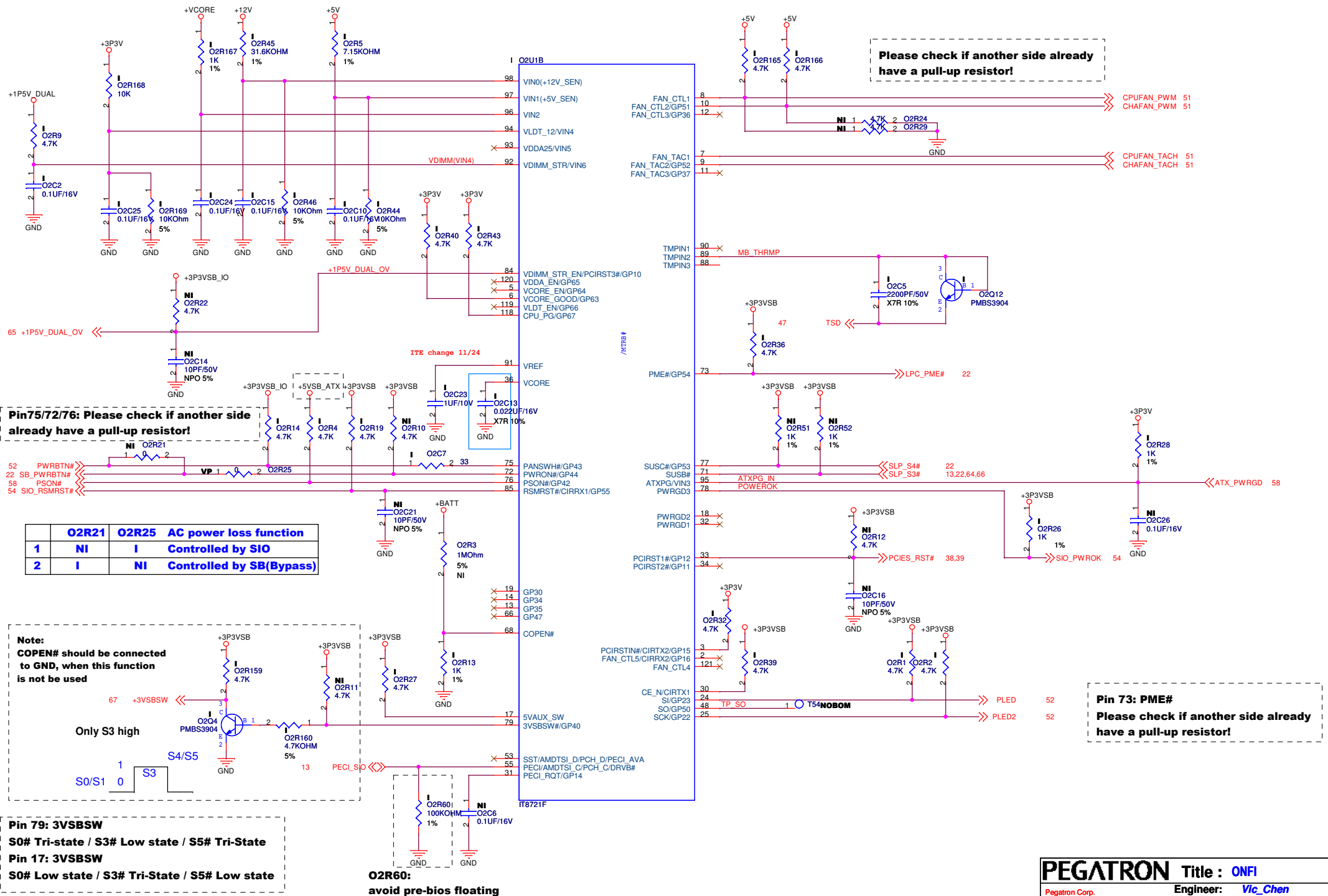
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SIO NCT5571D**

Engineer: **Vic Chen**

Pegatron Corp. Project Name **IPMIP-DP** Rev **1.01**

Date: **Wednesday, April 07, 2010** Sheet **47** of **68**



SM BUS Control

To PCH, PCI, and PCIE Slot

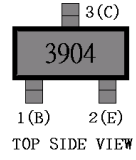
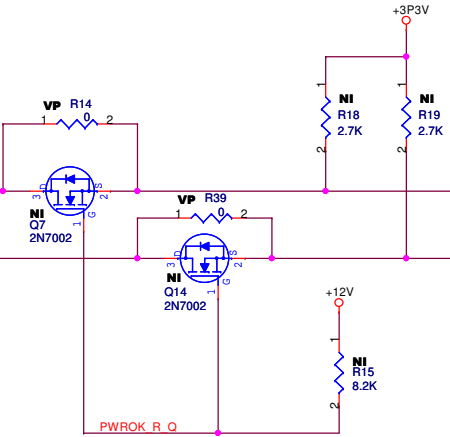
18,19,38,39,40,41,50 SMB_DATA_R

18,19,38,39,40,41,50 SMB_CLK_R

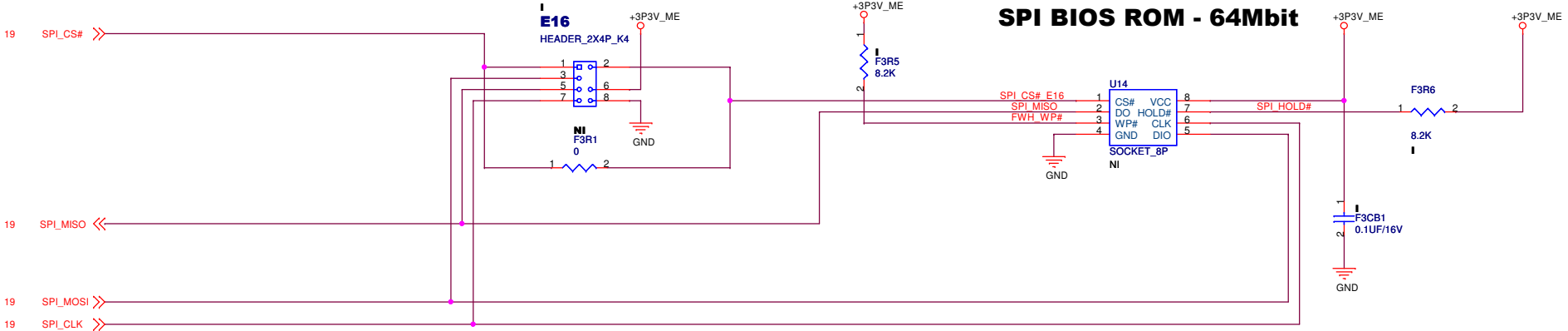
To Clock Gen, DIMMs, and ITP Debug Port

SMB_DATA_M 8,16,17,57

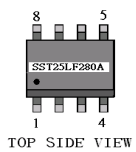
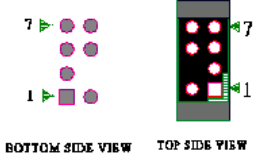
SMB_CLK_M 8,16,17,57

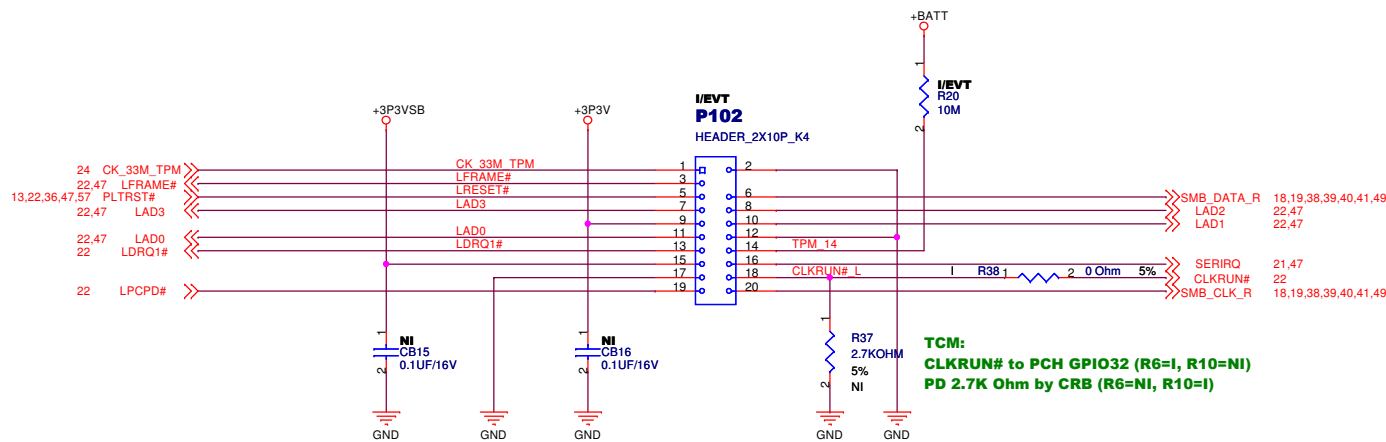


SPI BIOS ROM - 64Mbit



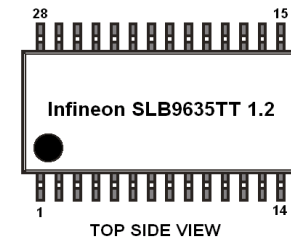
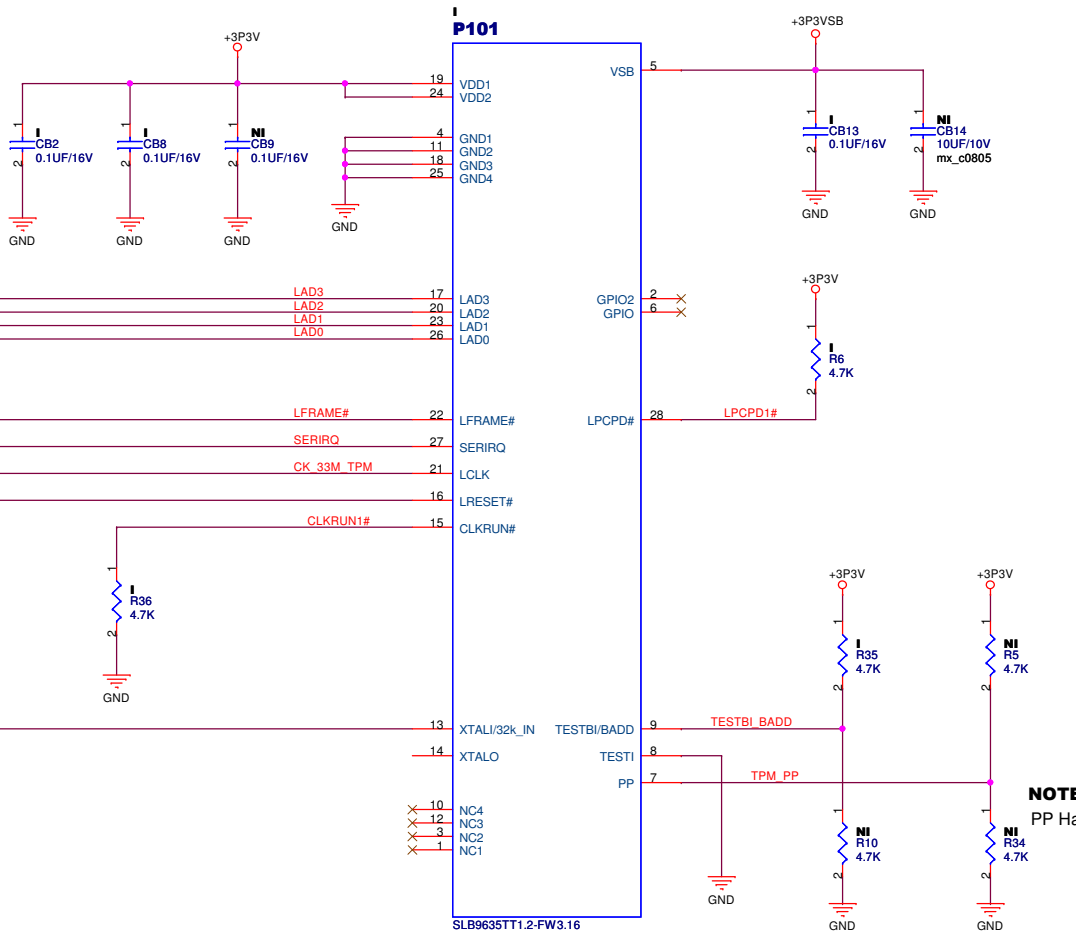
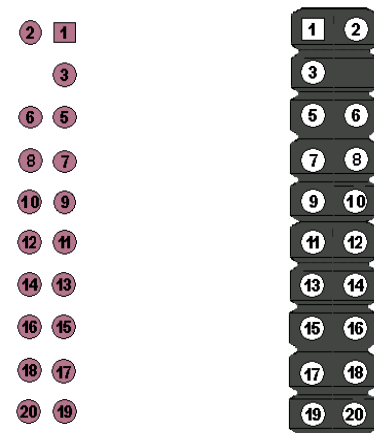
IPMIP-GS Change SPI to 64Mb
64Mb: 05X00Z2GE330
32Mb: 05X00Z2FC330
16Mb: 05X00Z2EA330





BOTTOM SIDE VIEW

TOP SIDE VIEW



NOTE:

TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

NOTE:

PP Have internal PULL-DOWN

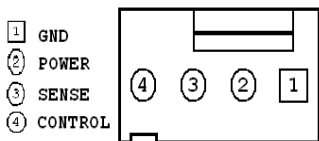
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA2 & TPM/TCM

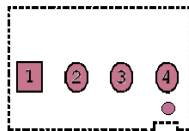
Pegatron Corp. Engineer: Vic_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 50 of 68



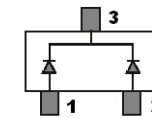
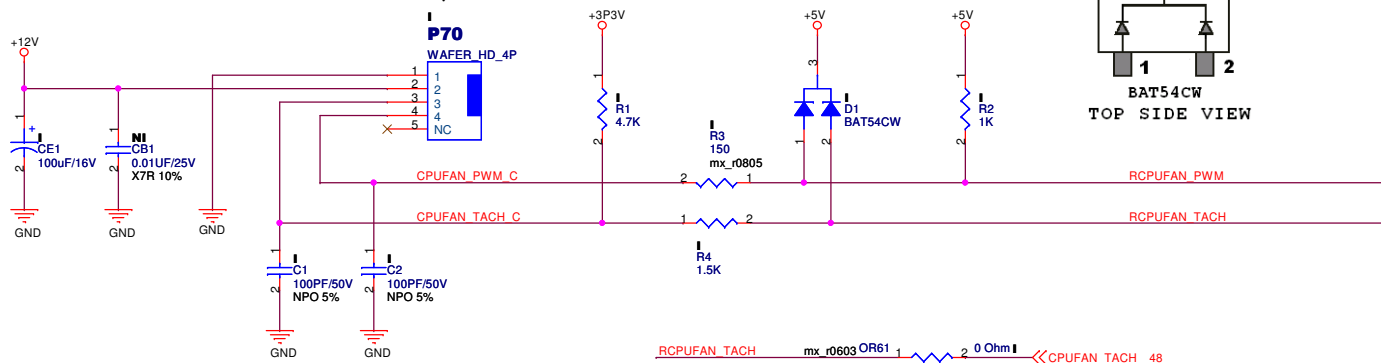
TOP SIDE VIEW



BOTTOM SIDE VIEW

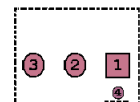
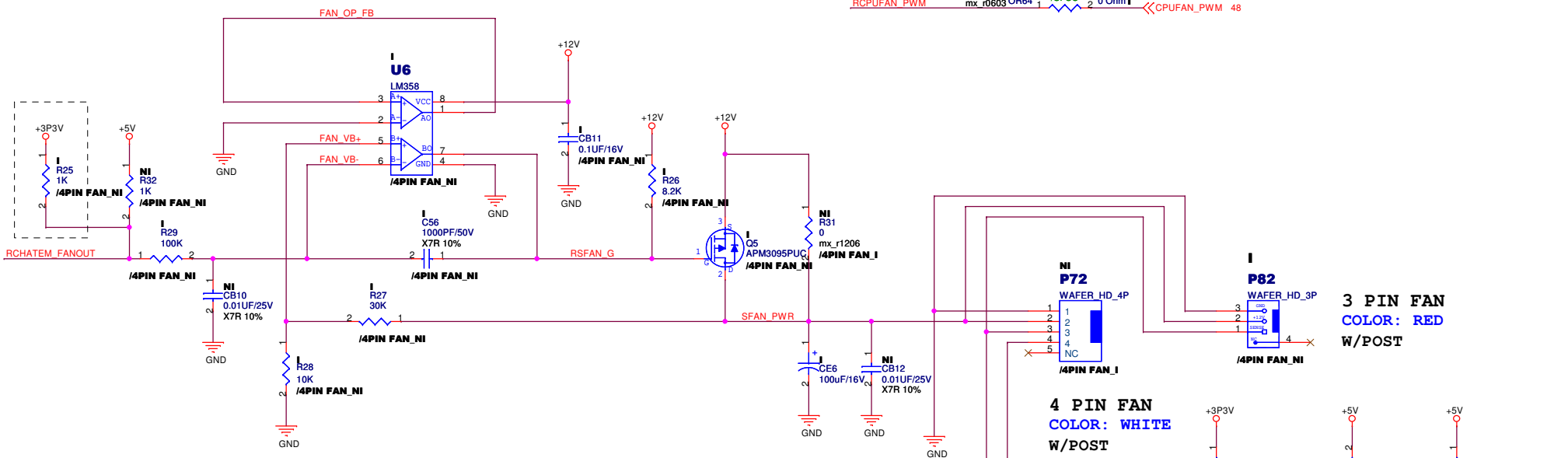
CPU FAN
COLOR: WHITE
W/POST

P70
WAFER_HD_4P

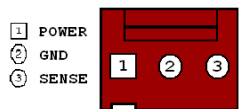


TOP SIDE VIEW

3 & 4 PIN CO-LAYOUT Circuit (Default 3 pin fan)



BOTTOM SIDE VIEW



TOP SIDE VIEW

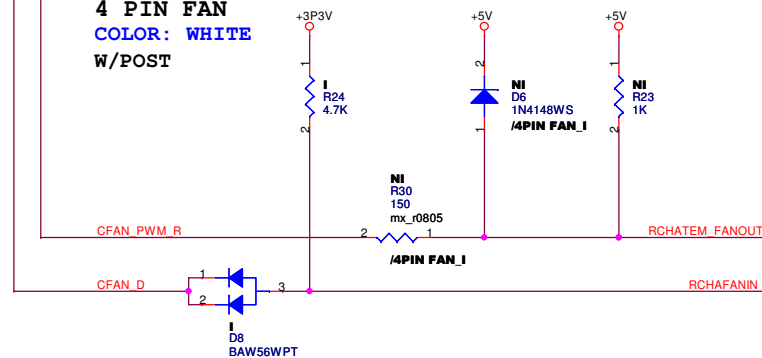
3 PIN FAN
COLOR: RED
W/POST

P72
WAFER_HD_4P

4 PIN FAN
COLOR: WHITE
W/POST

P82
WAFER_HD_3P

3 PIN FAN
COLOR: RED
W/POST

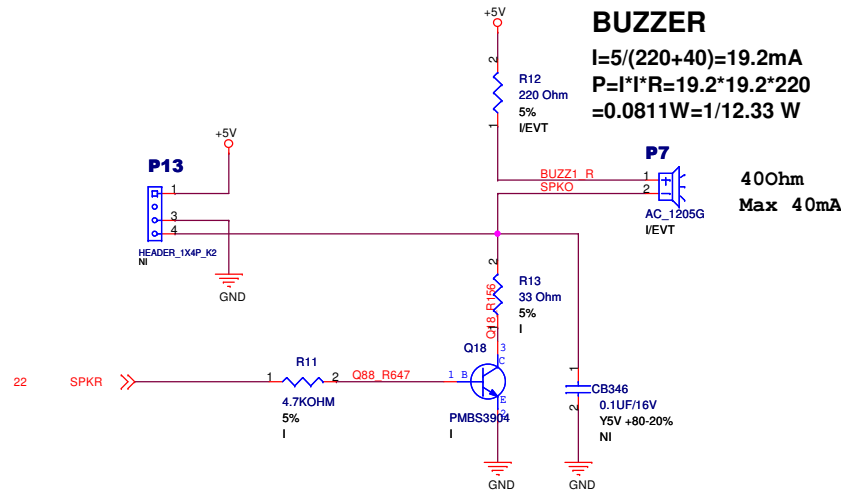
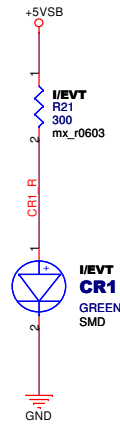


PEGATRON DT-MB RESTRICTED SECRET

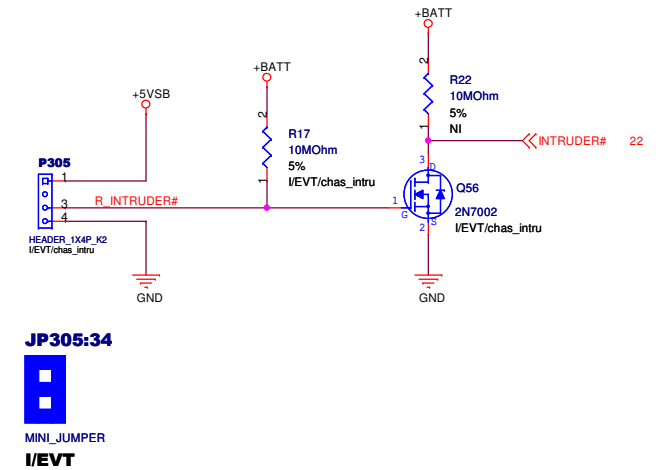
PEGATRON Title : 4-PIN FAN CONN

Pegatron Corp.		Engineer: Vic_Chen	
Size A3	Project Name	IPMIP-DP	Rev 1.01
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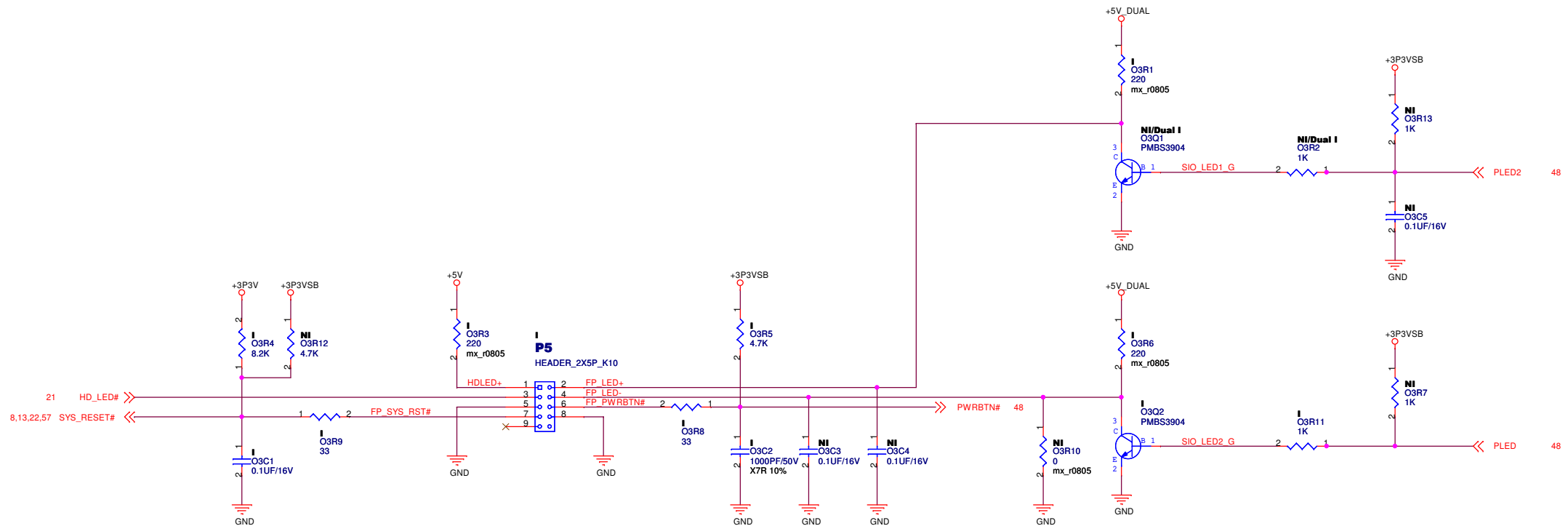
+5VSB : GREEN



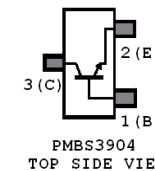
INTRUDER



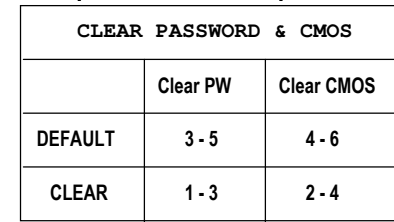
HPD CONTROL PANEL / LED CIRCUITRY



FRONT POWER LED COLOR SUPPORT	O3Q1	O3R2			
SINGLE COLOR	NI	NI			
DUAL COLOR	I	I			



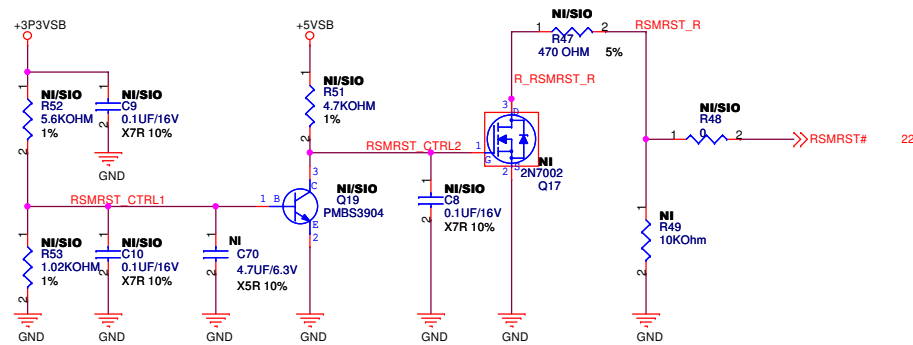
CLEAR CMOS & PASSWORD



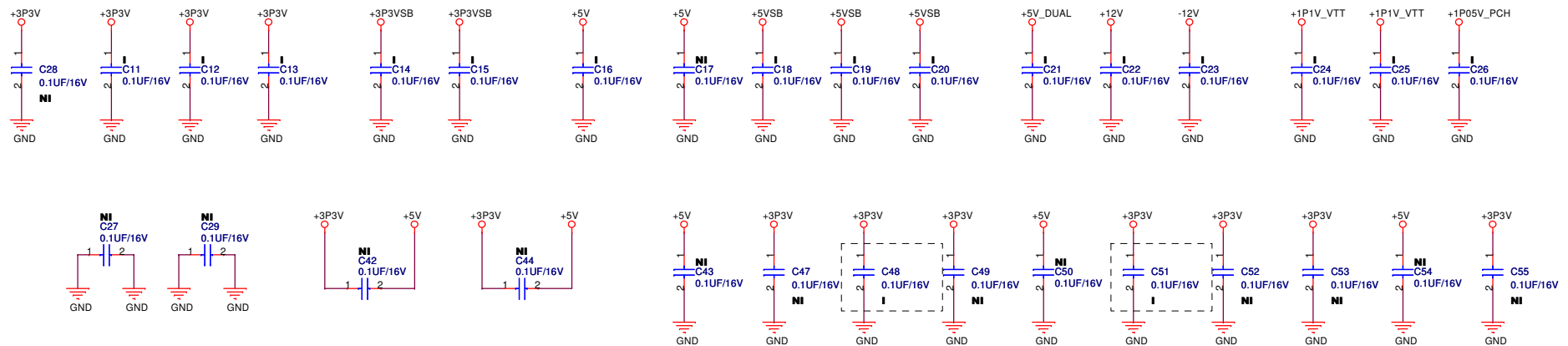
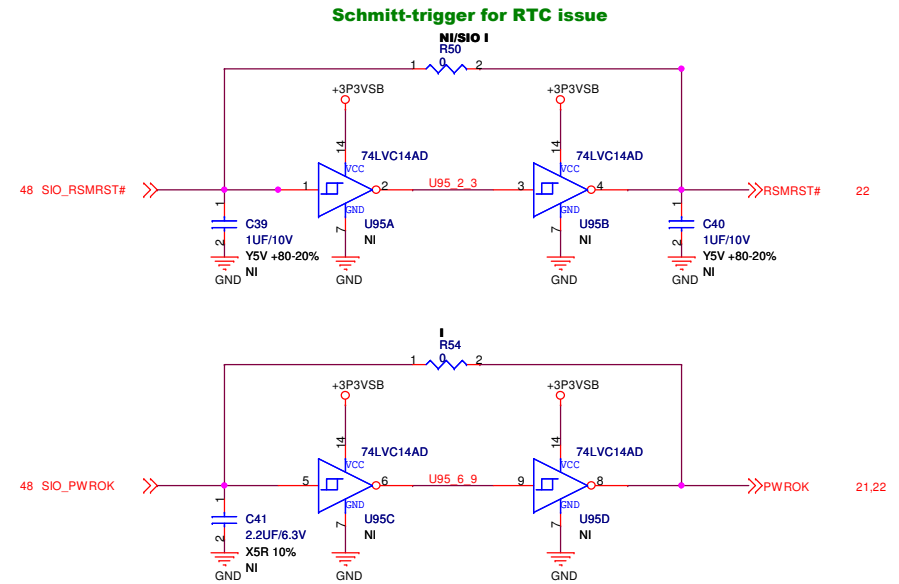
PEGATRON Title : **RTC / CMOS / KBMS**

Pegatron Corp.		Engineer: <i>Vic_Chen</i>	
Size A3	Project Name IPMIP-DP	Rev 1.01	
Date: <i>Wednesday, April 07, 2010</i>		Sheet <i>53</i> of <i>68</i>	

RSMRST CIRCUIT



10/02/01 Modify
1.Q17,3904 to 2N7002 (0201change)
2.R52,pull high form +5VSB to +3P3VSB
3.R51,pull high from +3P3VSB to +5VSB
4.Add,C70



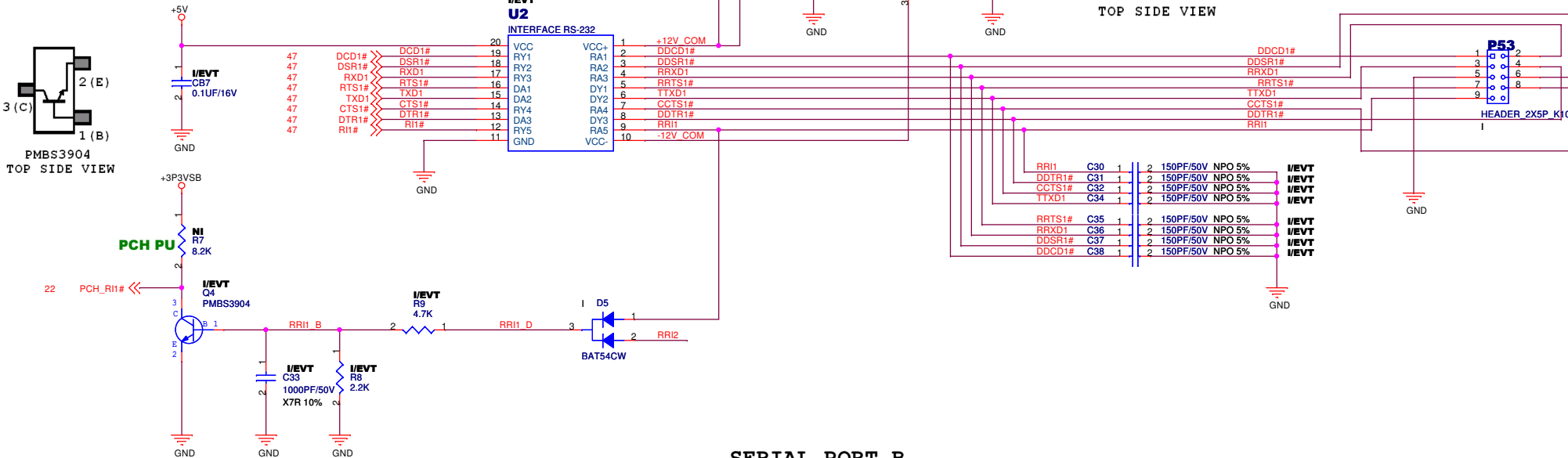
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **RSMRST CIRCUIT**

Pegatron Corp. **Engineer:** *Vlc_Chen*

Size	Project Name	Rev
A3	IPMIP-DB	1.01

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!!!!!!COM2 PIN NOT DECIDE

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title **ED/COM/SPKR/INTRU**

Pegatron Corp. Engineer: **Vlc_Chen**

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A diagram of a 60-pin connector. The pins are arranged in two rows of 30 pins each. The right row is numbered 1 to 31, and the left row is numbered 2 to 30. The connector is shown in a perspective view, with the pins protruding from a central body.

IPT1

Left pins (top to bottom):
 9 BPM0#
 7 BPM1#
 6 BPM2#
 4 BPM3#
 3 BPM4#
 1 BPM5#
 13 H_PRDY#
 13 H_PREQ#
 13 CK_ITP
 13 CK_ITP#
 13 H_TAPPWRGOOD
 8,16,17,49 SMB_CLK_M
 8,16,17,49 SMB_DATA_M
 28 NC
 14 VTT
 BtoB_CON_31P
 NI

Right pins (top to bottom):
 23 TDO
 29 TDI
 31 TMS
 30 TCK
 25 TRST#
 PWRGOOD
 RESET#
 DBR#
 RESERVED
 GND1
 GND5
 GND2
 GND6
 GND7
 GND3
 GND4
 GND8

External components and connections:
 - +1P1V_VTT supply connected to VTT pin (14) and pull-up resistors (NI GR17 1.5K, NI GR14 4.7K).
 - NI GR9 0 capacitor connected to SMB_CLK_M and SMB_DATA_M.
 - NI GR13 0 capacitor connected to SMB_CLK_M and SMB_DATA_M.
 - NI GCB2 0.1UF/16V capacitor connected to VTT and GND.
 - NI GR11 1K resistor connected to PWRGOOD and H_TAPPWRGOOD (13).
 - NI GR10 1K resistor connected to PWRGOOD and CPUPWRGD (13,22).
 - NI GR8 1K resistor connected to RESET# and H_RSTOUT# (13).
 - NI GR12 0 resistor connected to DBR# and SYS_RESET# (8,13,22,52).
 - NI GR15 1K resistor connected to RESERVED and PLTRST# (13,22,36,47,50).
 - Dashed box labeled "Place near cpu" containing NI GR8, NI GR12, and NI GR15.

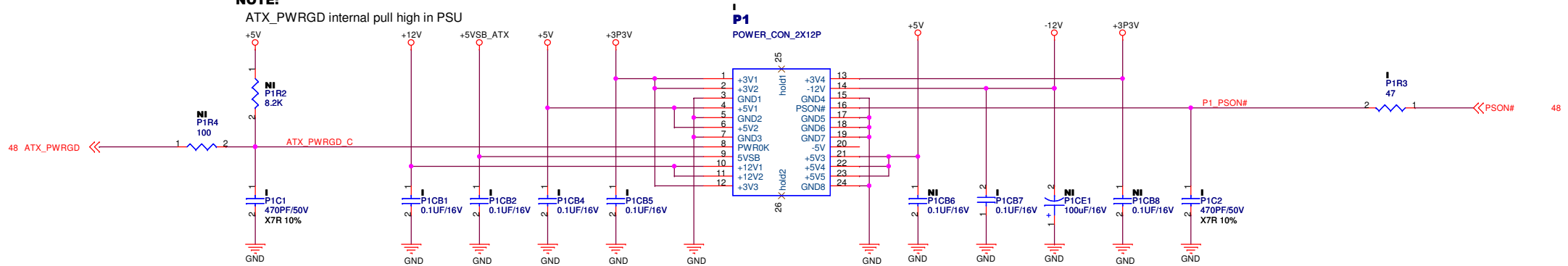
ASUS P/N: 12G161300310 => HRS/DF9C-31

ASUS P/N: 12G161300310 => HRS/DF9C-31S-1V(22)

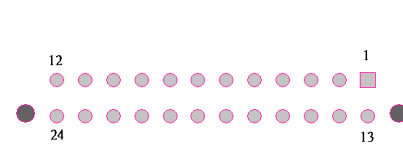
ATX POWER_24P SUPPLY CONNECTOR

NOTE:

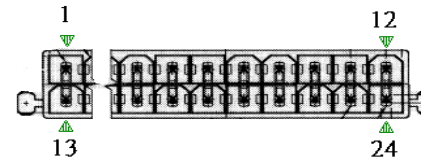
ATX_PWRGD internal pull high in PSU



All of the Caps Around the ATX Power Connector



BOTTOM SIDE VIEW

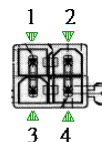
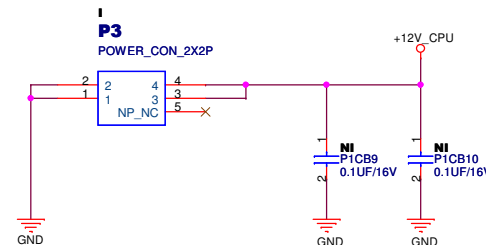


TOP SIDE VIEW

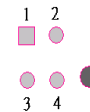
PCB

PCB38
IPMIP-GS R1.00 RED
08M1-0UX0200

VRM POWER_4P SUPPLY CONNECTOR



TOP SIDE VIEW



BOTTOM SIDE VIEW

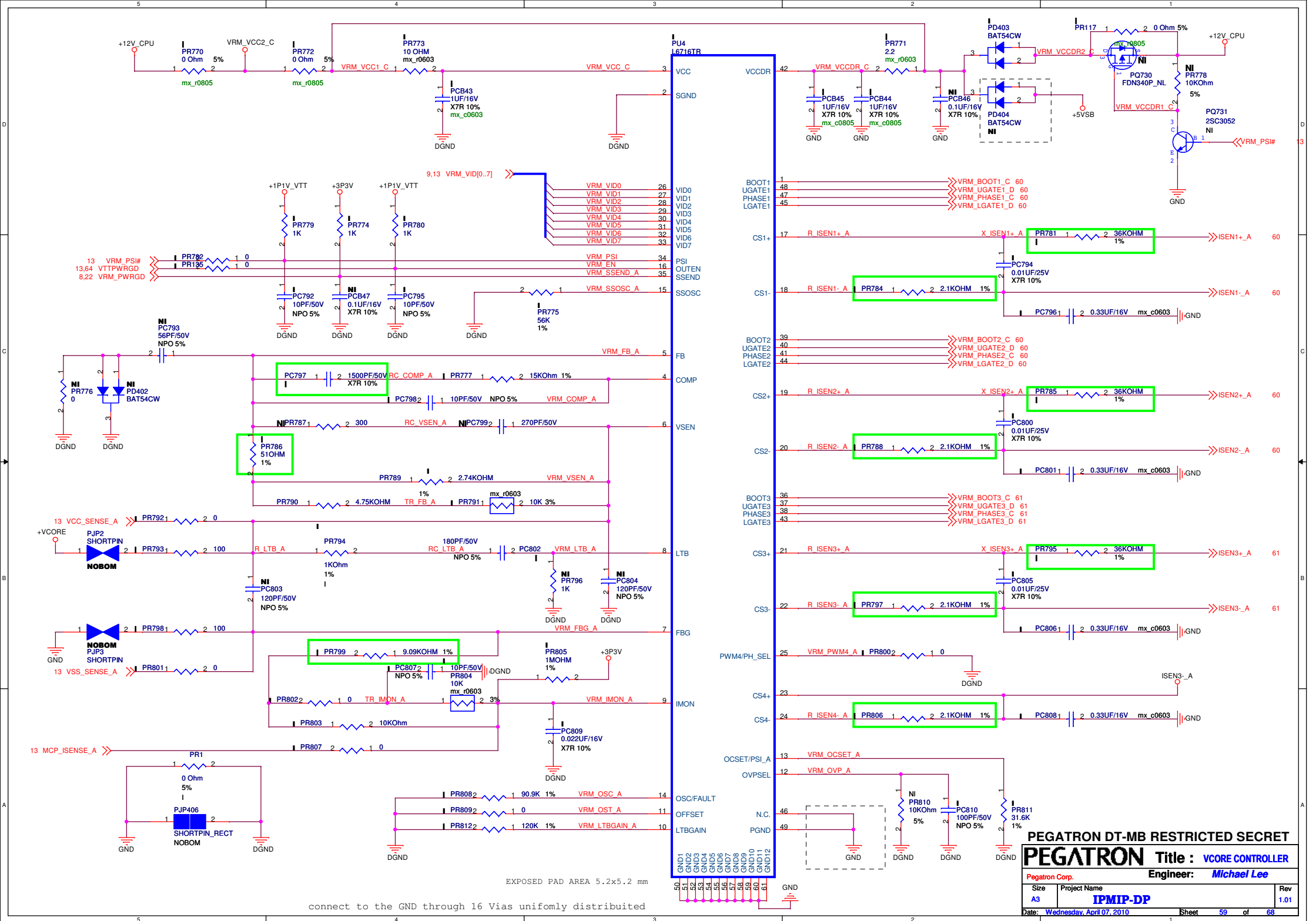
PEGATRON DT-MB RESTRICTED SECRET

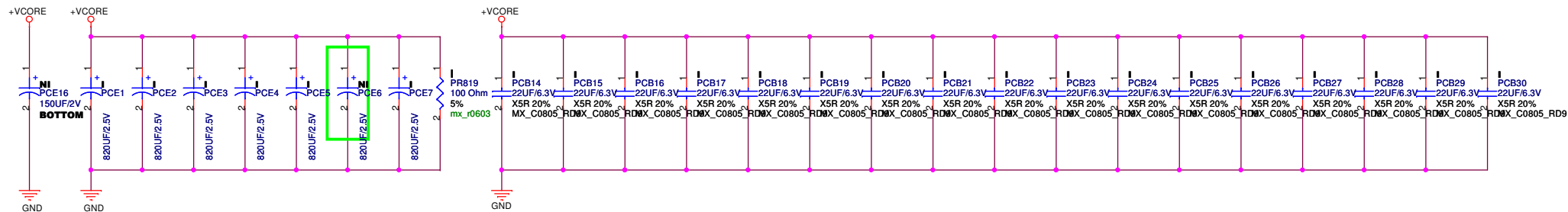
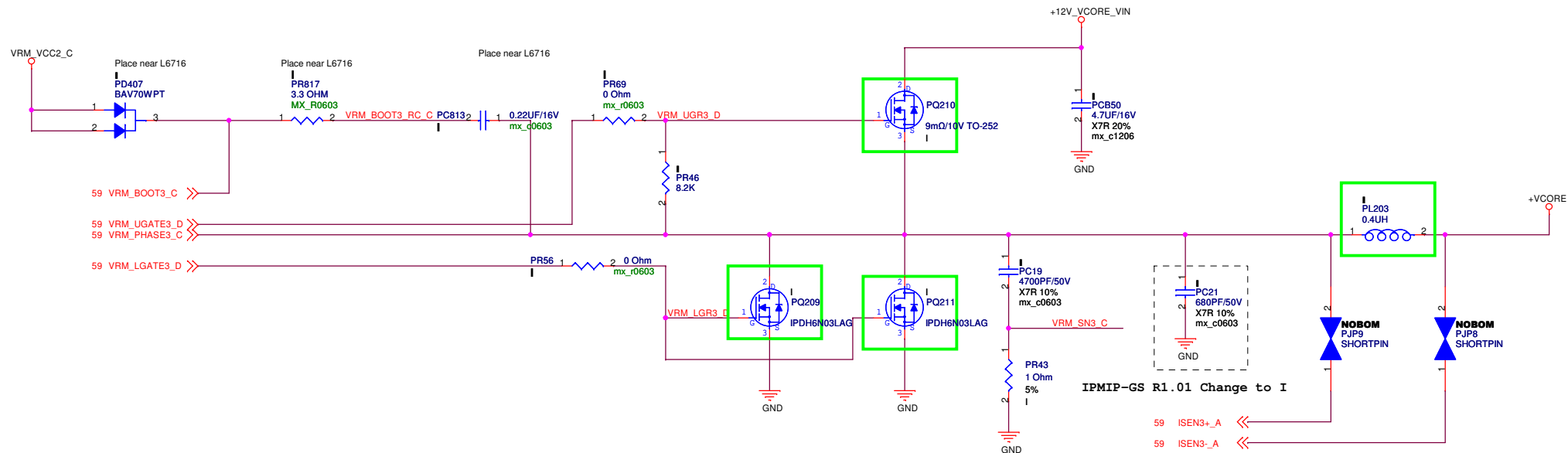
PEGATRON Title : **ATX POWER**

Pegatron Corp. Engineer: **Vic_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

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+CPU Vcore OUTPUT CAPs

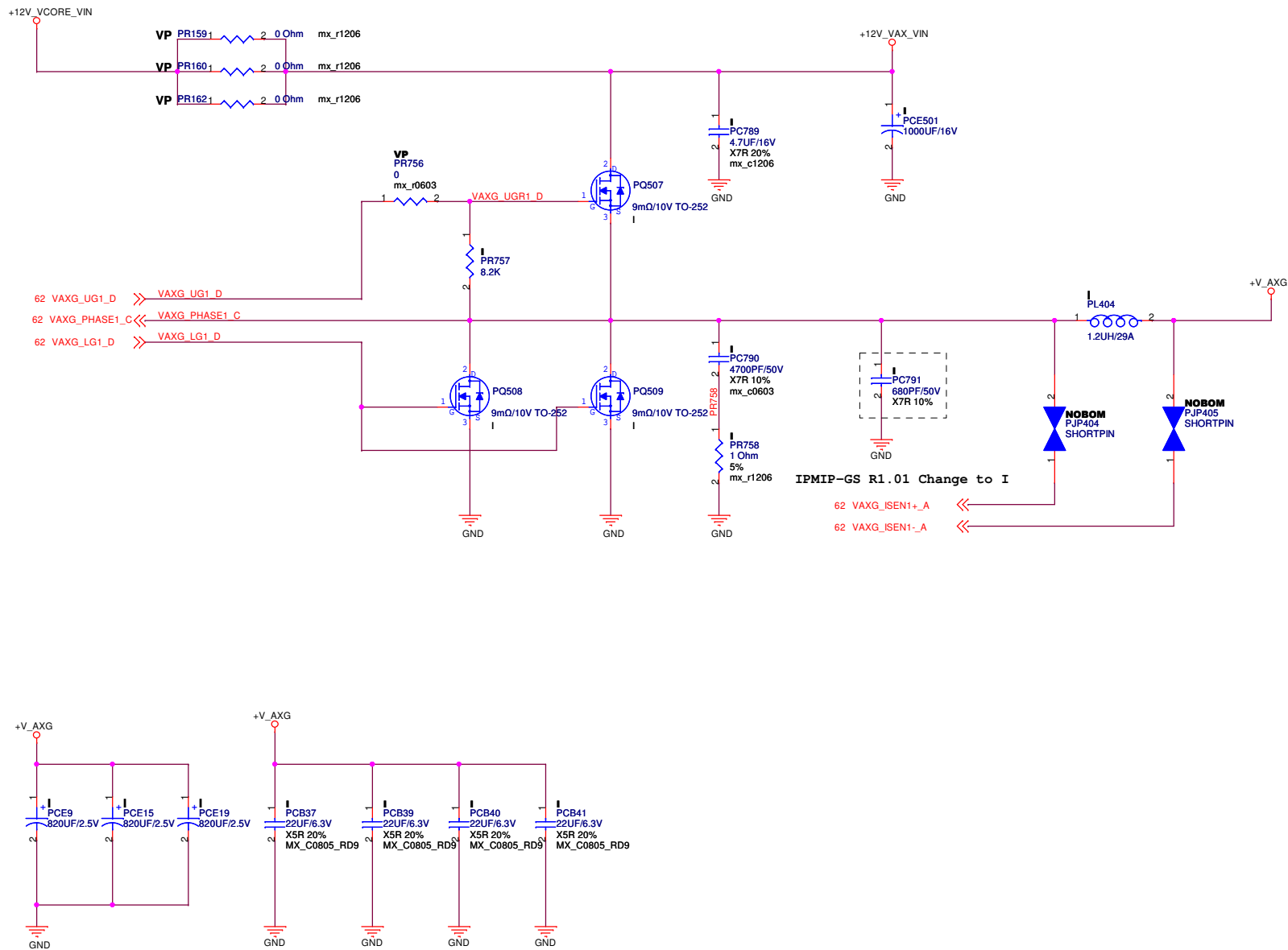
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Vcore DRIVER-2

Pegatron Corp. Engineer: Michael Lee

Size A3	Project Name IPMIP-DP	Rev 1.01
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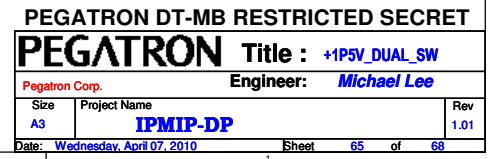
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **VAGX DRIVER**

Pegatron Corp. Engineer: **Michael Lee**

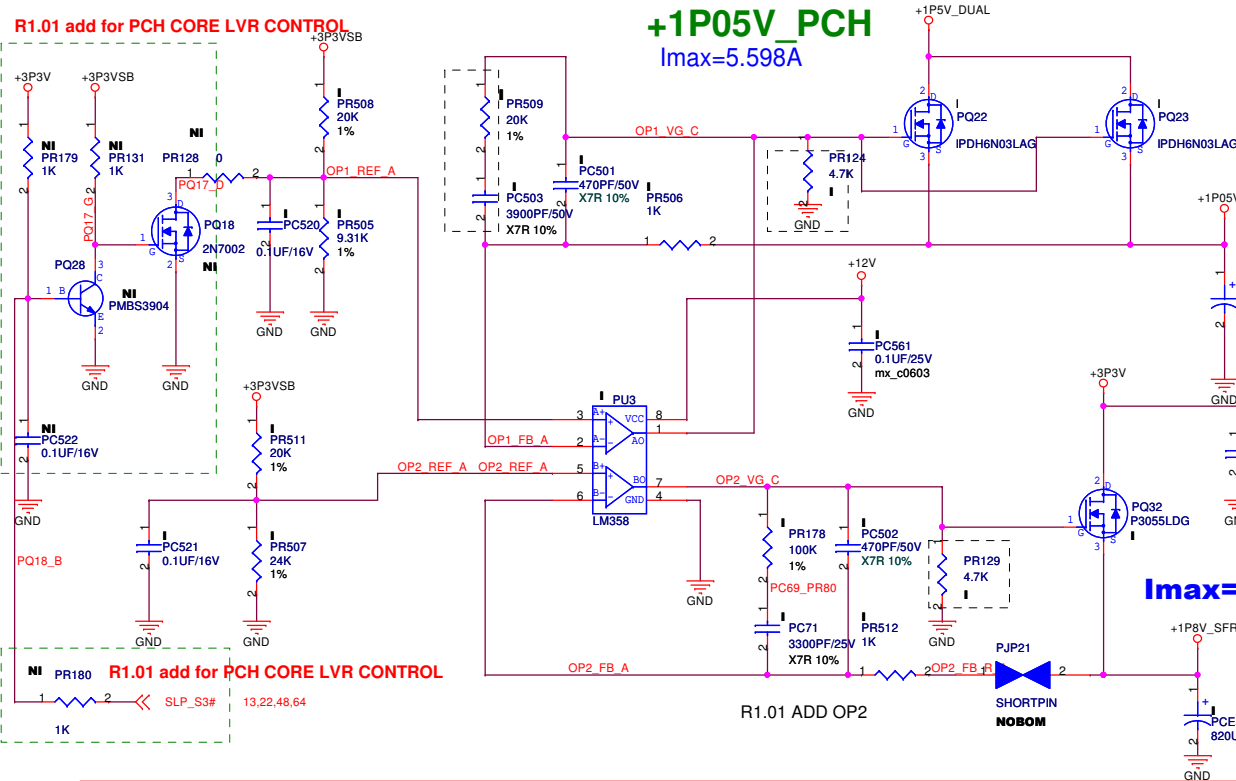
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$I_{max}=19.628A$

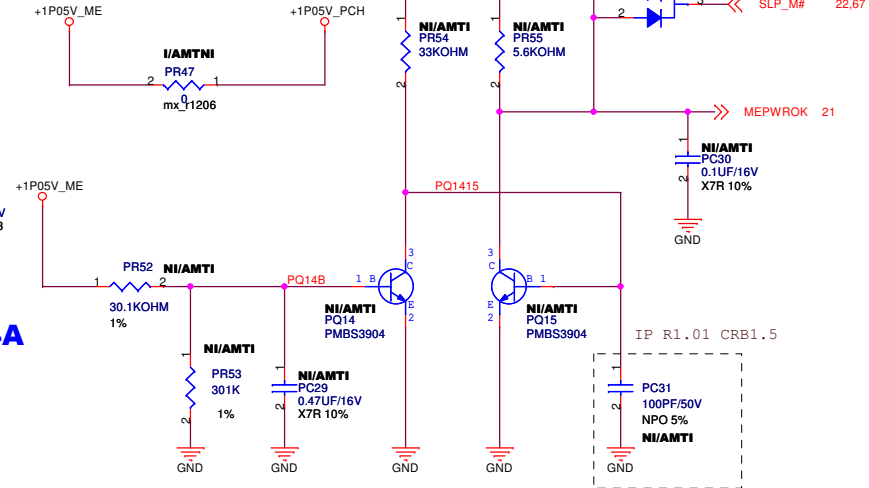


R1.01 add for PCH CORE LVR CONTROL

+1P05V_PCH
I_{max}=5.598A



Install for AMT support

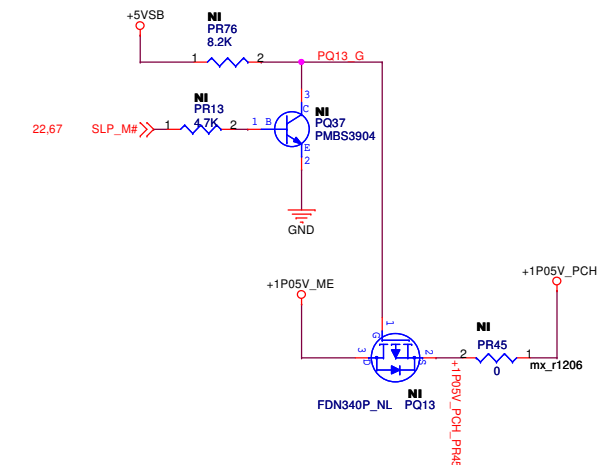
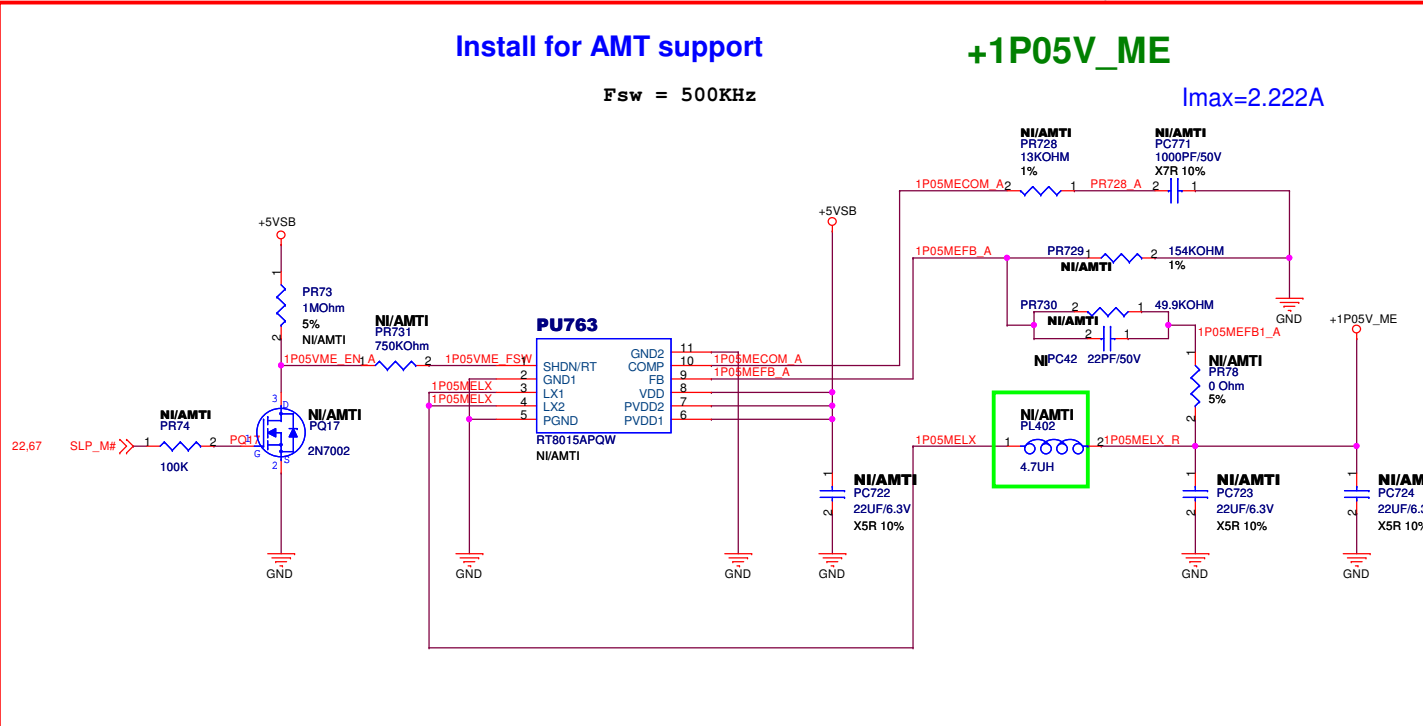


Install for AMT support

+1P05V_ME

F_{sw} = 500KHz

I_{max}=2.222A



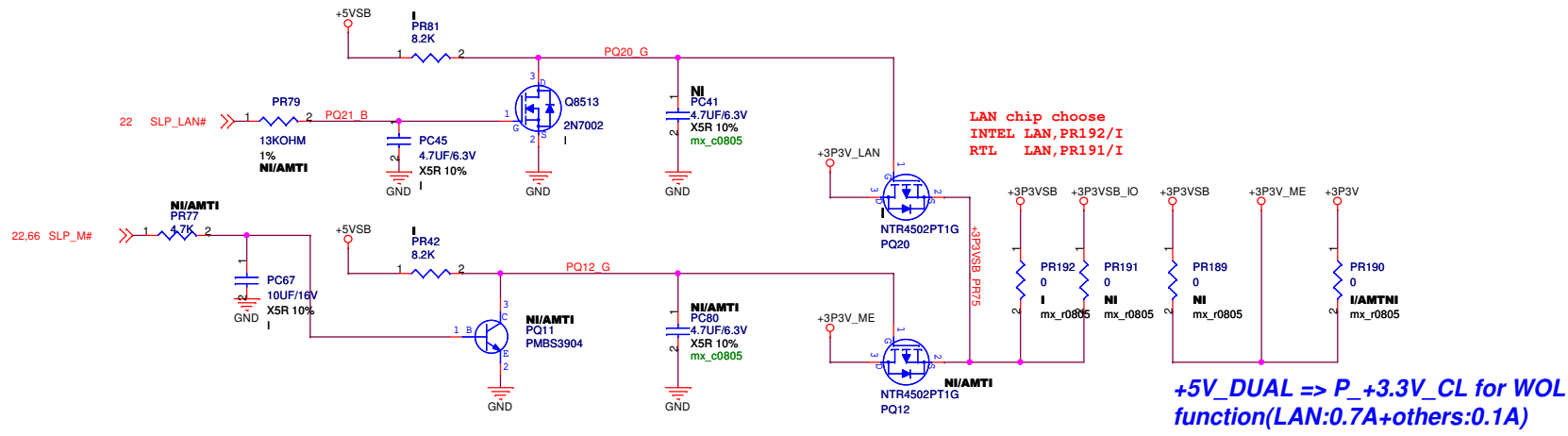
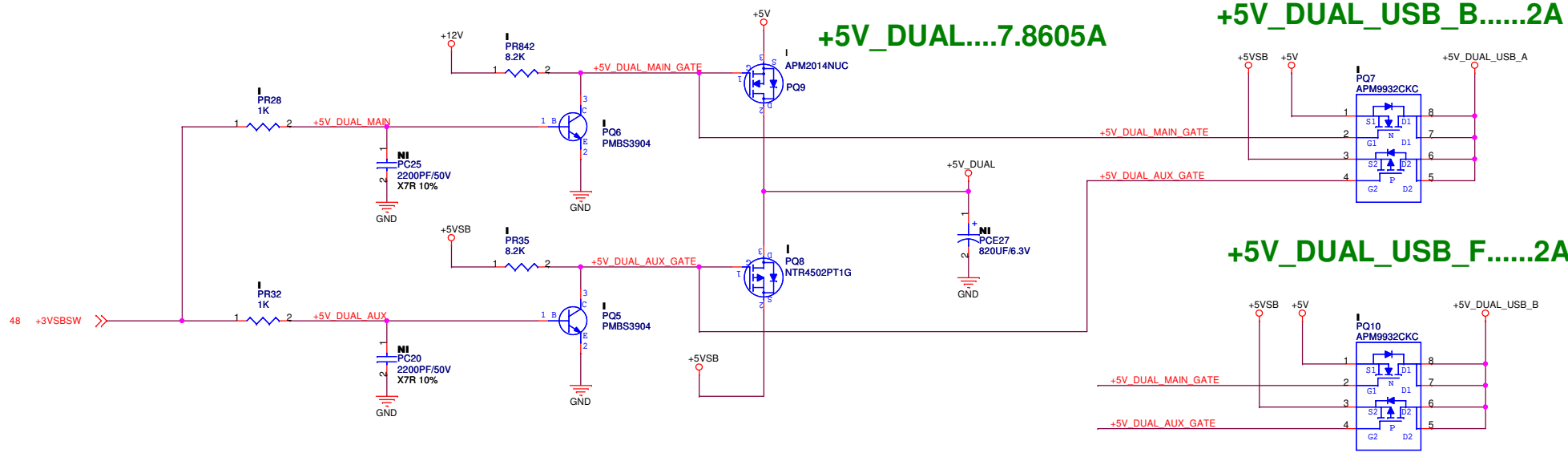
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title :+1P05V_PCH & +1P05V_ME

Pegatron Corp. Engineer: Michael Lee

Size A3 Project Name IPMIP-DP Rev 1.01

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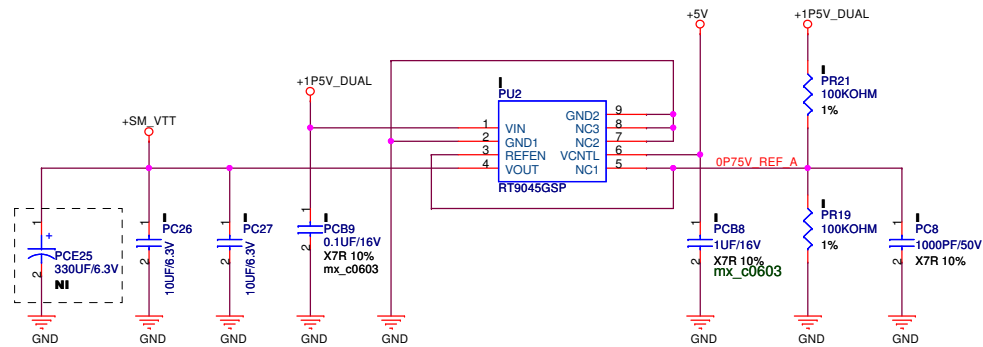


WOL_EN & SLP_M#:
For AMT
 1 S0/S1 S3 S4 S5
 0

WOL_EN & SLP_M#:
For non-AMT
 1 S0/S1 S3 S4 S5
 0

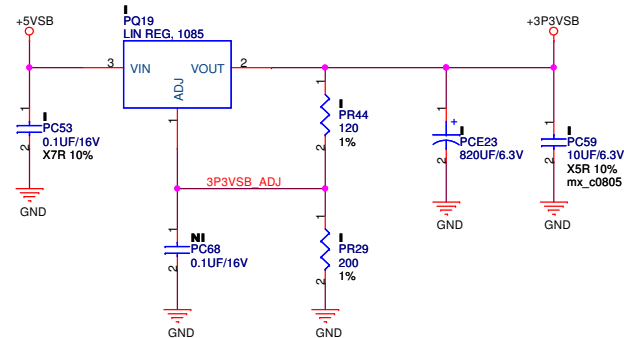
+1P5V_DUAL ==> +0P75V_VTT_DDR

$I_{max}=0.83A$



4/28 MODIFY

+5VSB ==> +3P3VSB....3.44A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title: **+0P75V_VTT_ & +1P8V_SFR**

Pegatron Corp. Engineer: **Michael Lee**

Size A3	Project Name IPMIP-DP	Rev 1.01
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